

Iris HSW/BDW Schematics

Broadwell-ULT

2015-01-20

REV : A00

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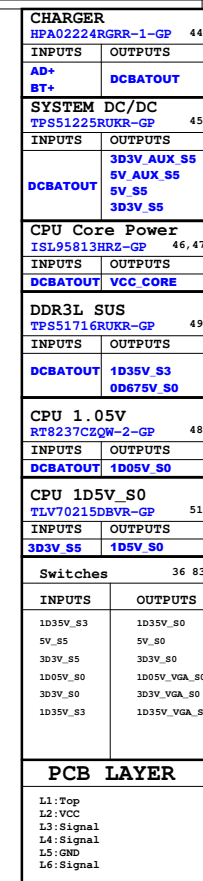
DY : None Installed


UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

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Iris2/Tulip/VanGogh Block Diagram



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Date:	Worksheets	Printed:	1/1	Sheet	2	of 102

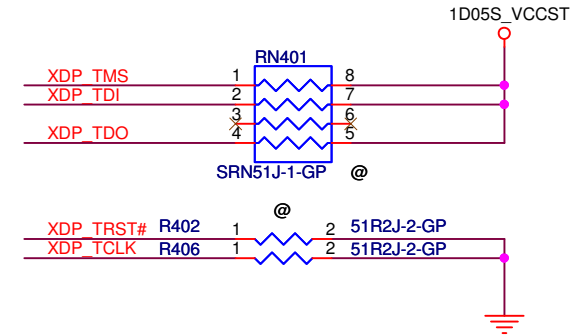
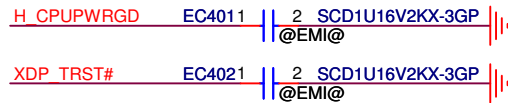
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						Date:		Wednesday, January 21, 2015		Sheet 3 of 102	

Main Func = CPU

For EMI Reserved



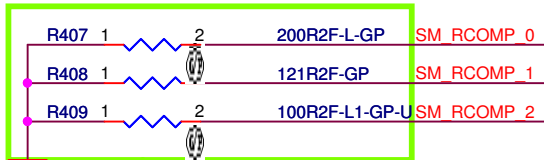
Layout Note:

Impedance control: 50 ohm

<24,42,43,48> H_PROCHOT# <<>>

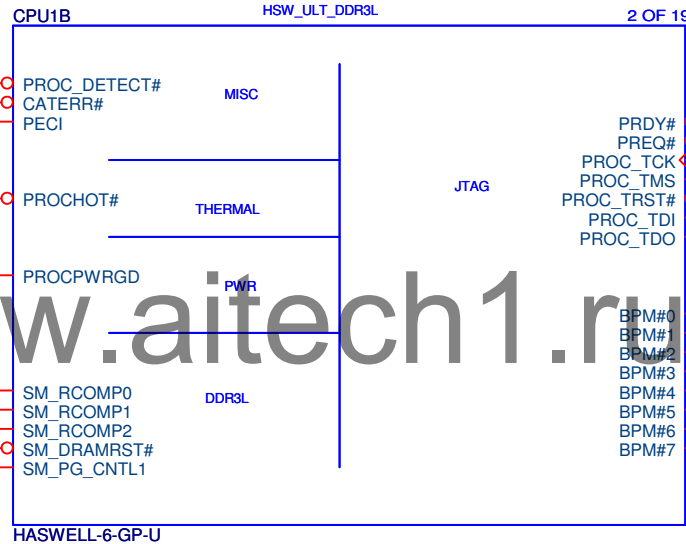
<36> H_THERMTRIP_EN <<<<

Layout Note: Close to CPU



Layout Note:

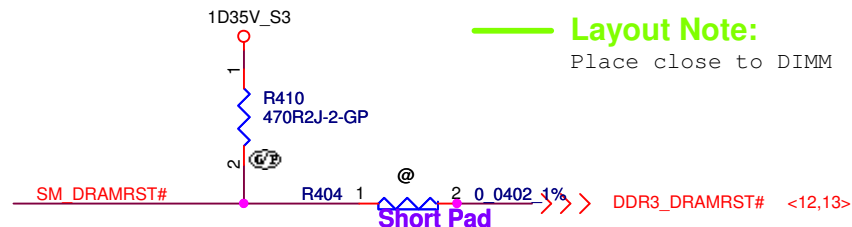
Design Guideline:
SM_RCOMP keep routing length less than 500 mils.



XDP_BPM[7:0] <<>> XDP_BPM[7:0] <96>

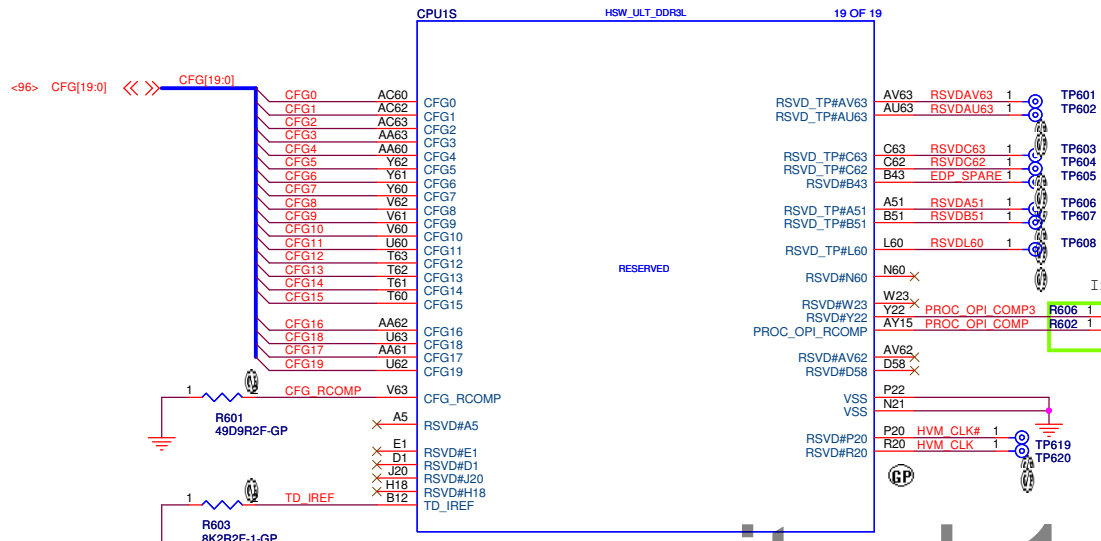
Layout Note:

Place close to DIMM



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Main Func = CPU



7.4 Reserved or Unused Signals

- The following are the general types of reserved (RSVD) signals and connection guidelines:
- RSVD - these signals should not be connected
 - RSVD_TP - these signals should be routed to a test point
 - RSVD_NCTF - these signals are non-critical to function and may be left unconnected

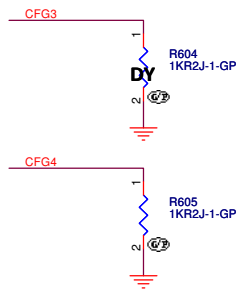
Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

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PCH strap pin:

Signal Name	Description	Direction / Buffer Type
CFG[19:0]	<p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate Platform Design Guide for pull-down recommendations when a logic low is desired.</p> <ul style="list-style-type: none">• CFG[2:0]: Reserved configuration lane. A test point may be placed on the board for these lanes.• CFG[3]: MSR Privacy Bit Feature<ul style="list-style-type: none">– 1 = Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting– 0 = IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden• CFG[4]: eDP enable<ul style="list-style-type: none">– 1 = Disabled– 0 = Enabled• CFG[19:5]: Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL

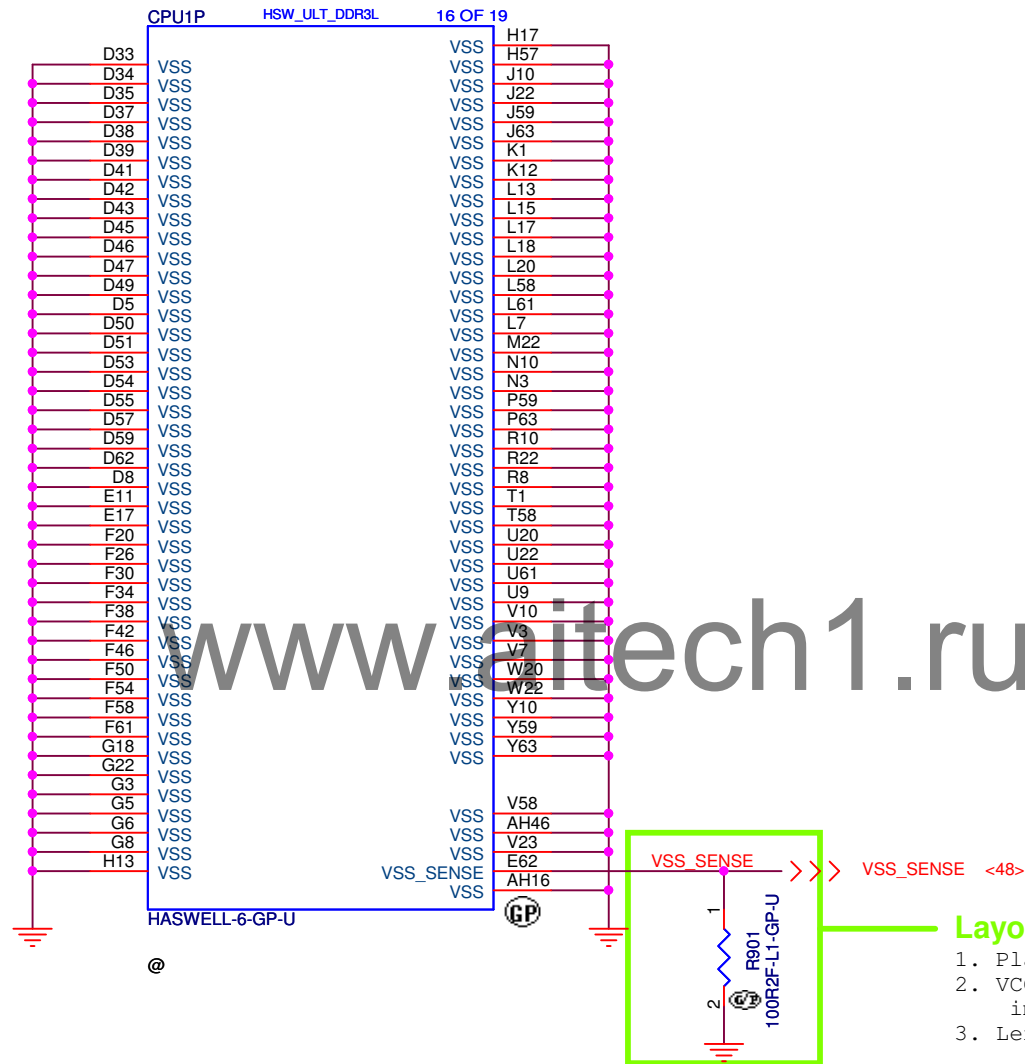


PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

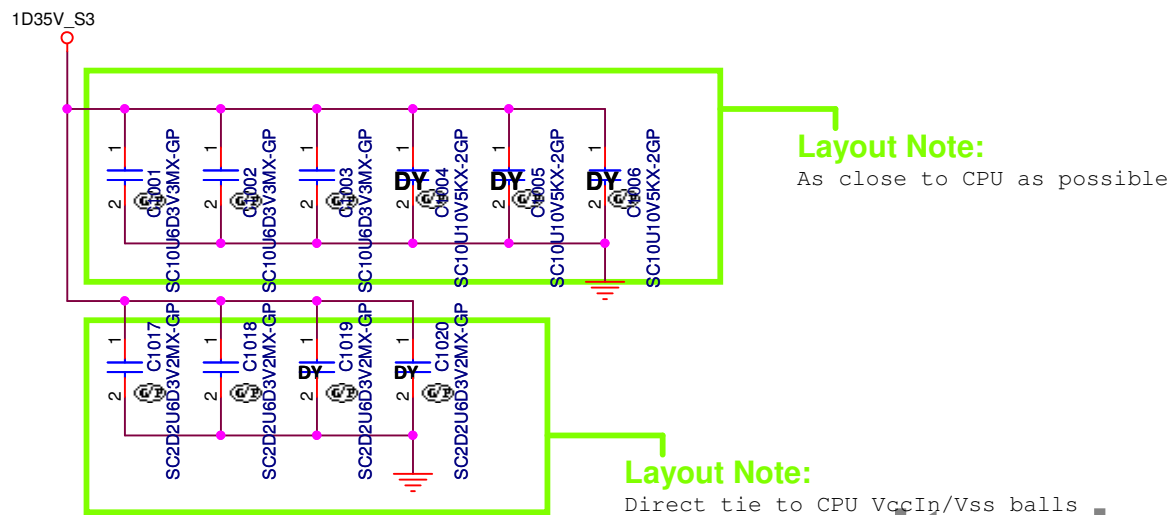
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Main Func = CPU



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Main Func = CPU

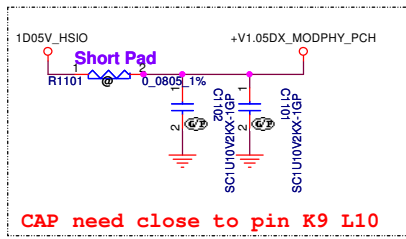


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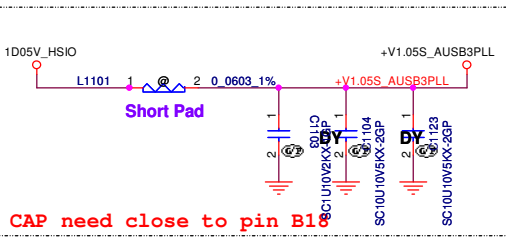
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MAX: 1.92A

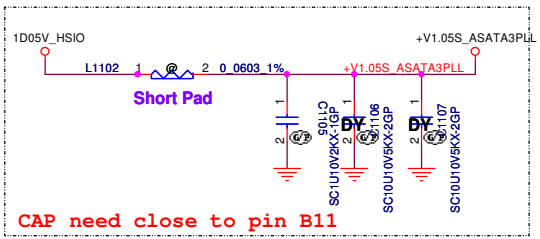
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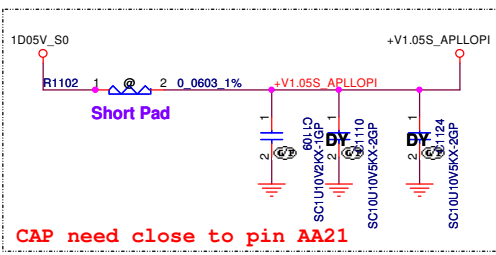
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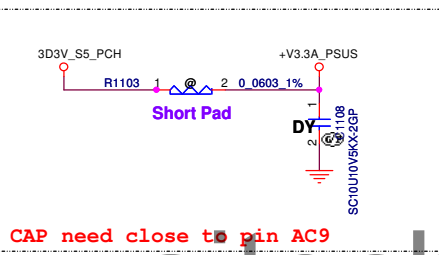
42mA



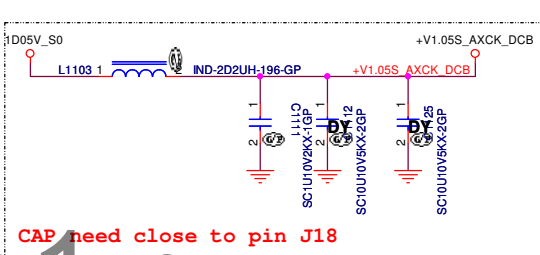
57mA



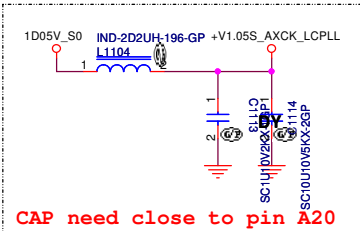
62mA



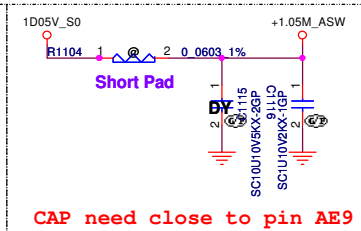
185mA



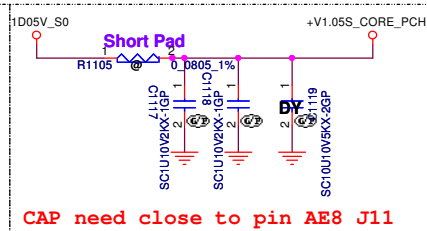
31mA



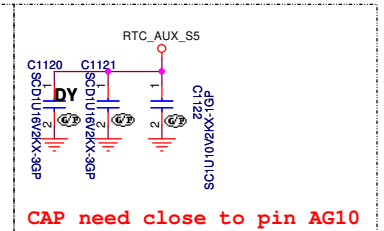
658mA

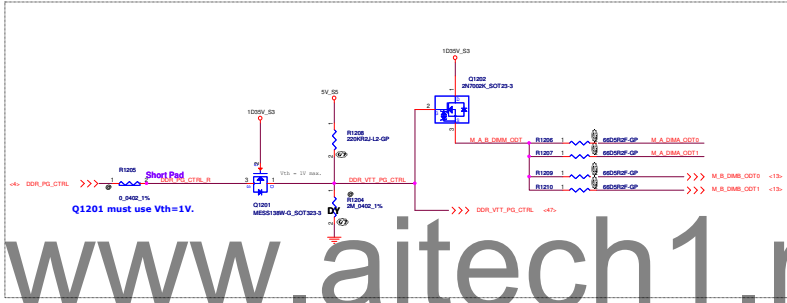


1.632A



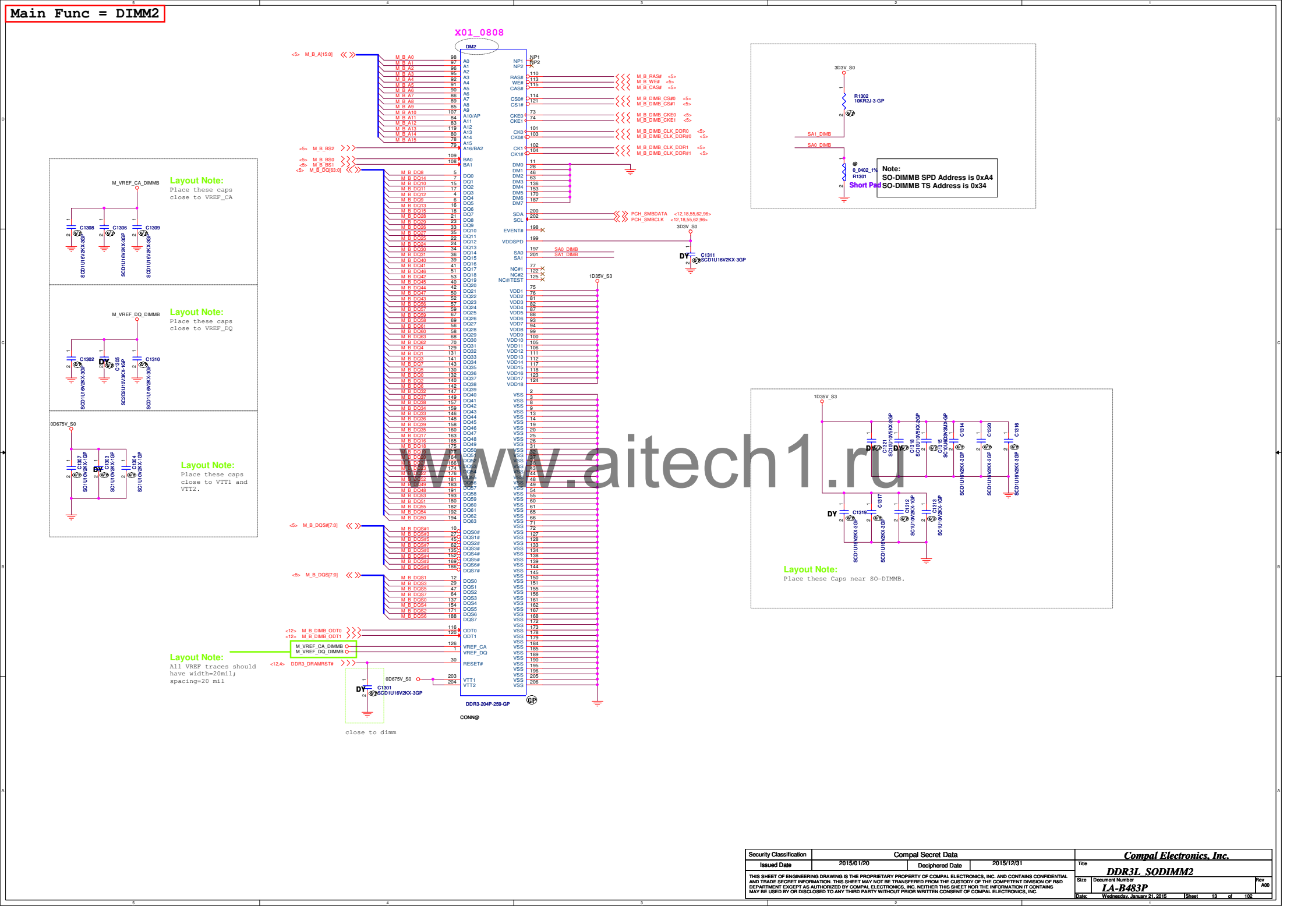
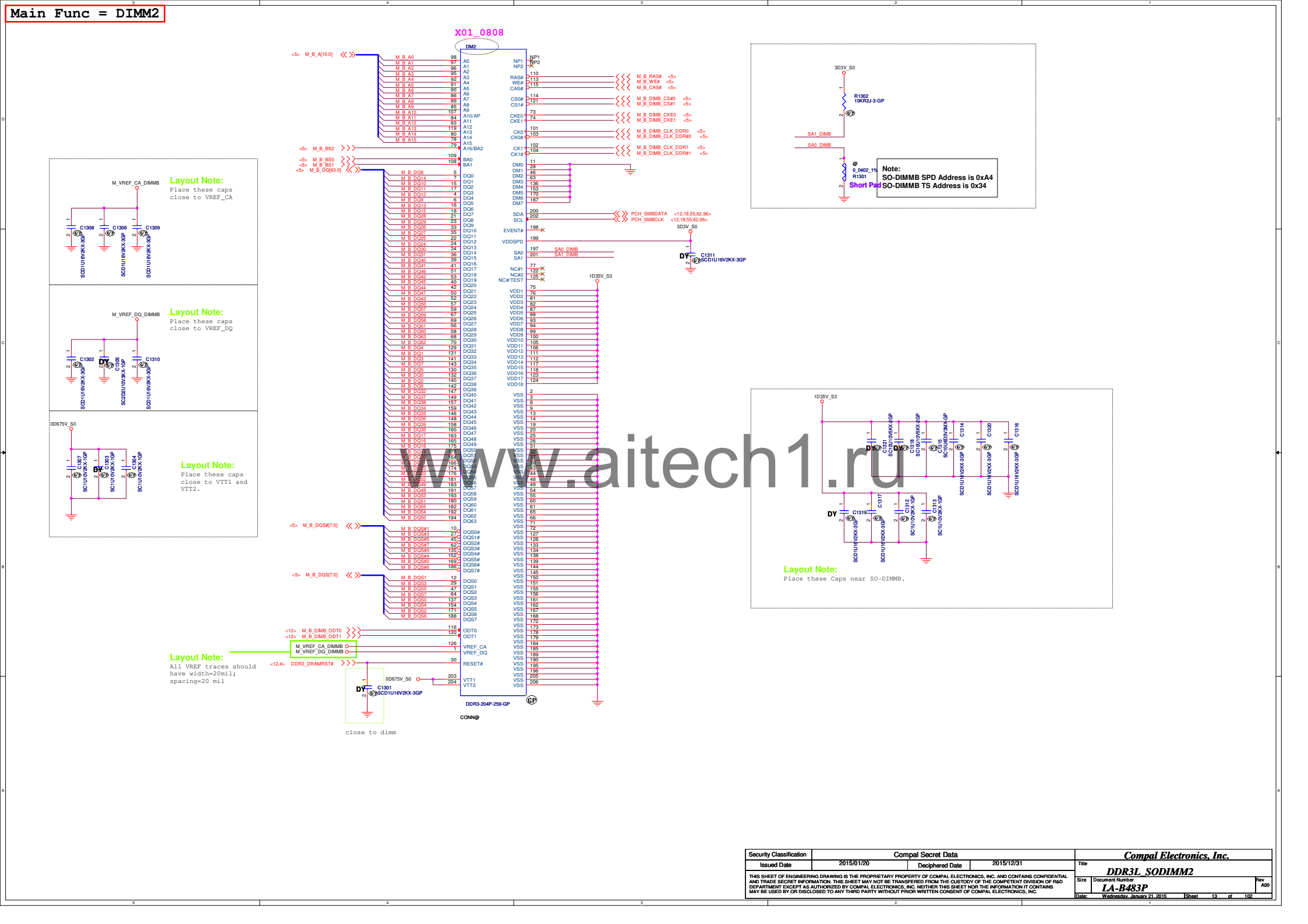
1mA





Q1201 must use V_{eh}=1V. by >>> DDR_VTT_P0_CTRL v4%

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Main Func = DIMM2

X01_0808

Layout Note:
Place these caps close to VREF_CA

Layout Note:
Place these caps close to VREF_DQ

Layout Note:
Place these caps close to VTT1 and VTT2.

Layout Note:
All VREF traces should have width=20mil; spacing=20 mil

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

Layout Note:
Place these Caps near SO-DIMMB.

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Title: **DDR3L SODIMM2**

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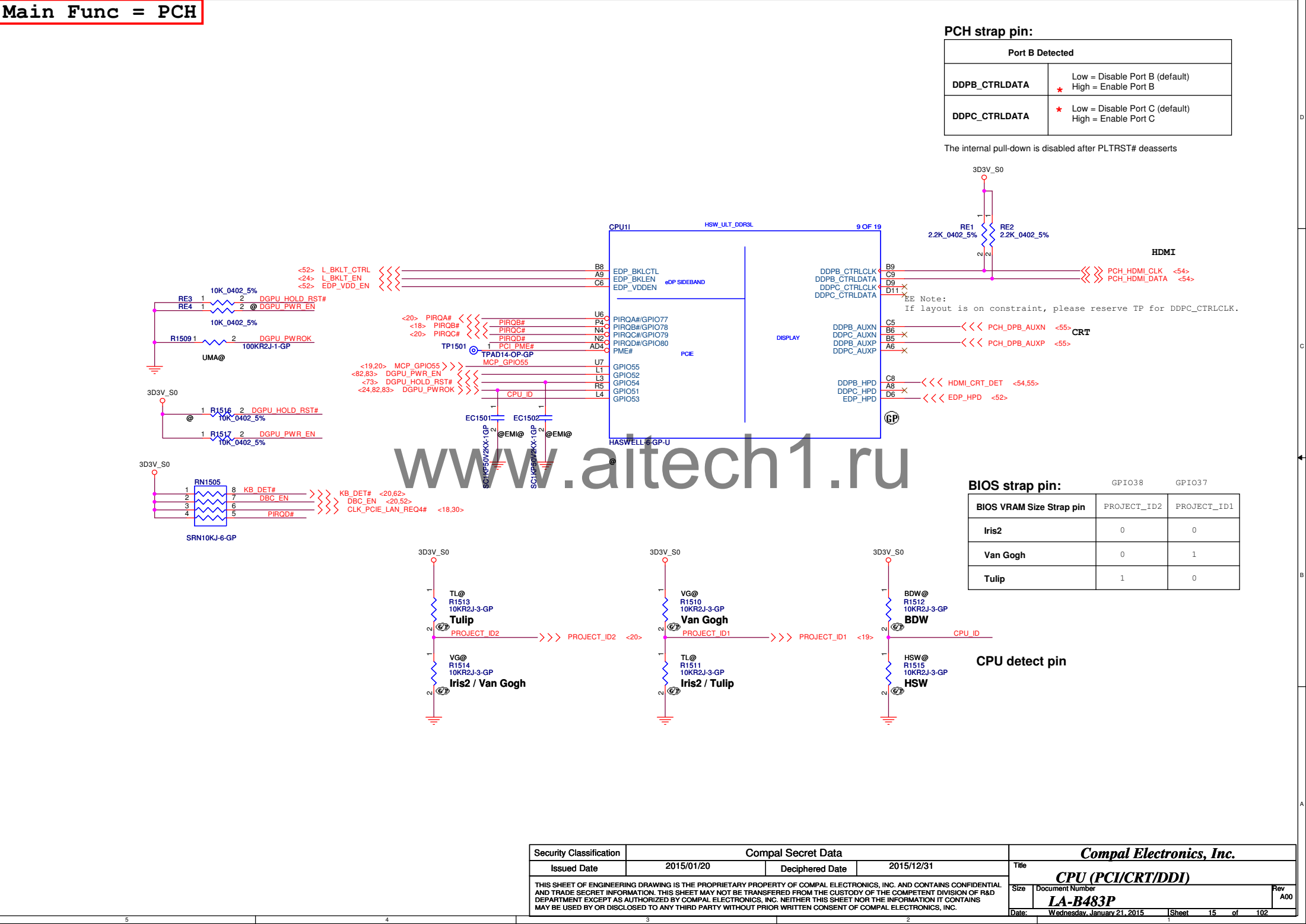
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						Size		Document Number		Rev	
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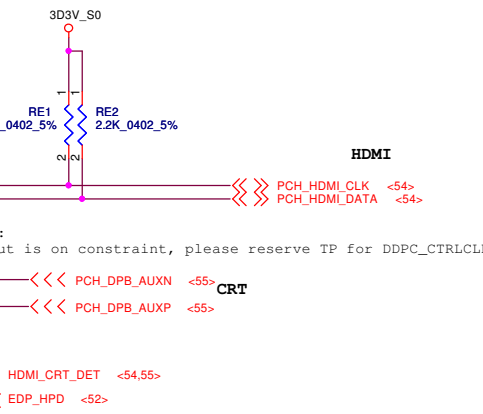
Main Func = PCH



PCH strap pin:

Port B Detected	
DDPB_CTRLDATA	★ Low = Disable Port B (default) High = Enable Port B
DDPC_CTRLDATA	★ Low = Disable Port C (default) High = Enable Port C

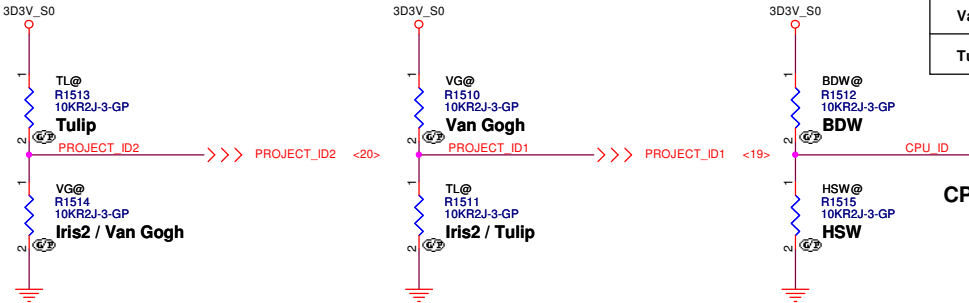
The internal pull-down is disabled after PLTRST# deasserts



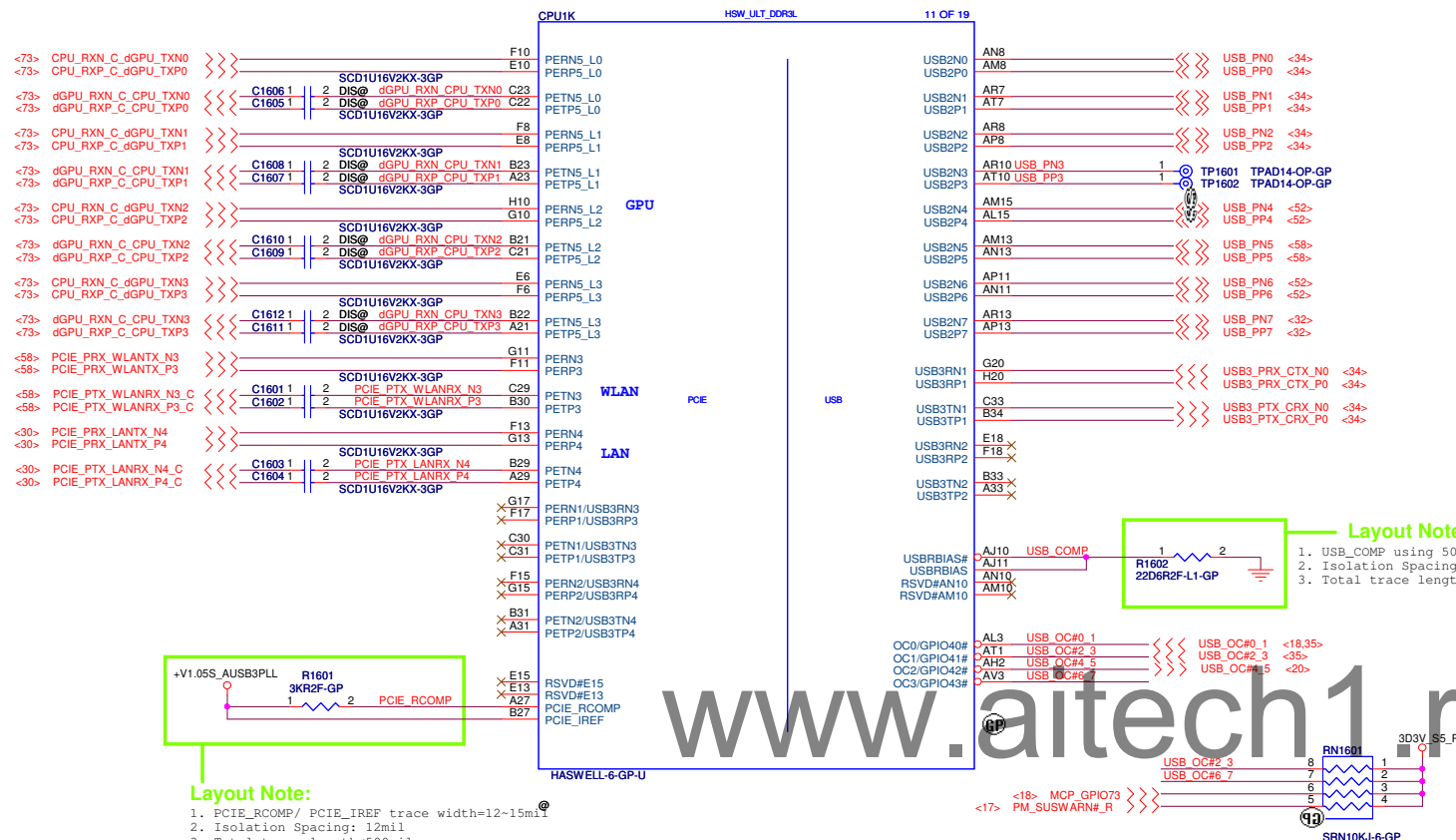
BIOS strap pin:

BIOS VRAM Size Strap pin	PROJECT_ID2	PROJECT_ID1
Iris2	0	0
Van Gogh	0	1
Tulip	1	0

CPU detect pin



Main Func = PCH



USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB2.0 Port2 (Debug Port/IOBD)
2	USB2.0 Port3 (IOBD)
3	X
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader

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PCIE Table

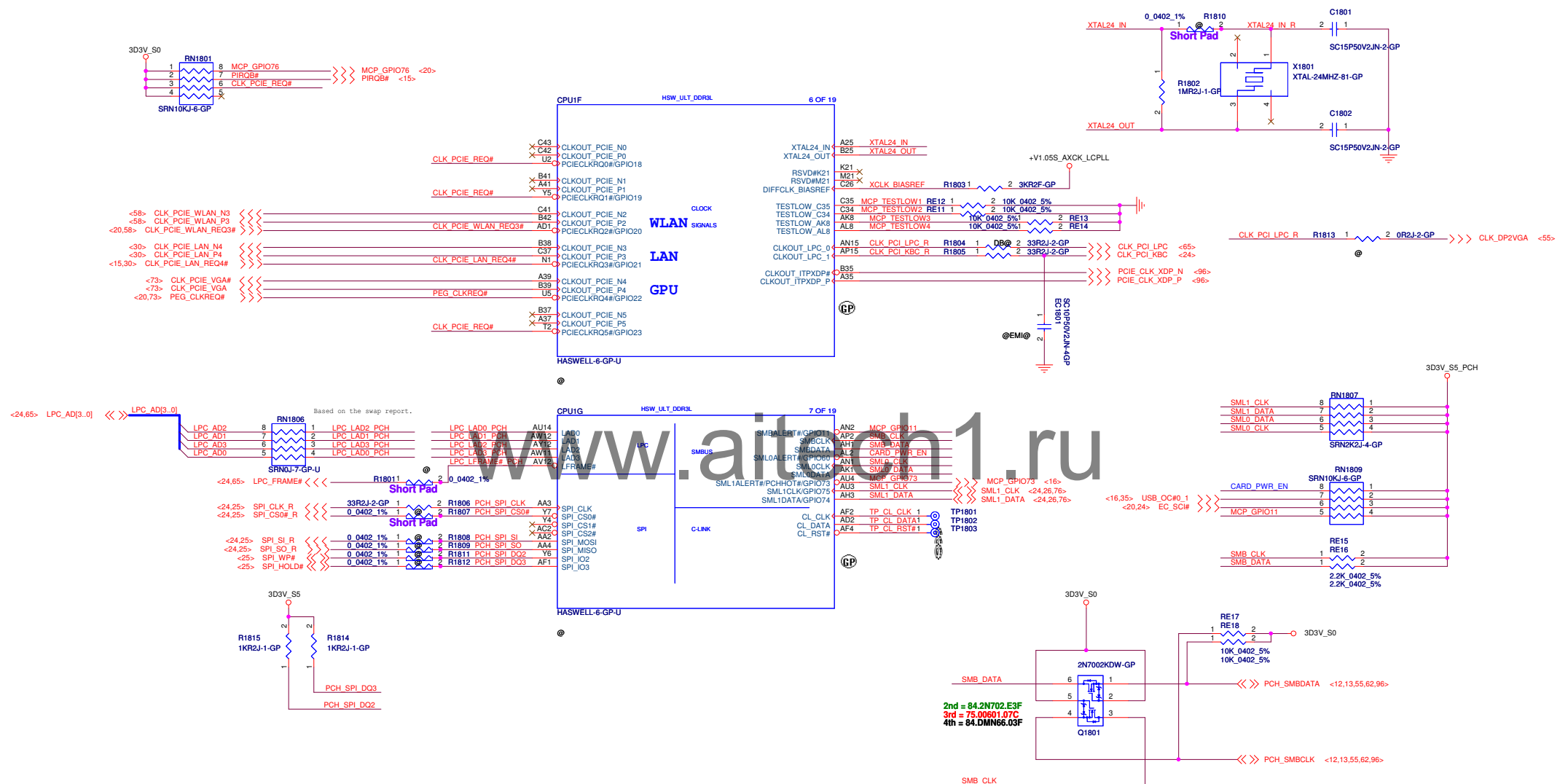
Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN	
5 (L0~L3)	GPU	
6 (L3)	HDD	SATA0
6 (L2)	ODD	SATA1
6 (L0~L1)	N/A	

#515621

Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0	PCIe* Port 5 Lane 1	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	SATA 6Gb/s Port 3	SATA 6Gb/s Port 2	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD			GPU	GPU	GPU	GPU	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	PCIe* Port 6 Lane 2	PCIe* Port 6 Lane 3
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD			GPU	GPU	GPU	GPU				

Main Func = PCH

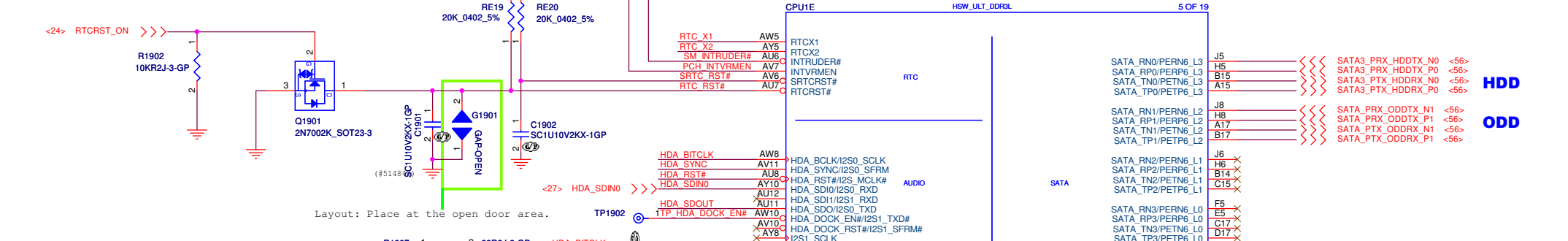


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Main Func = PCH

PCH strap pin:

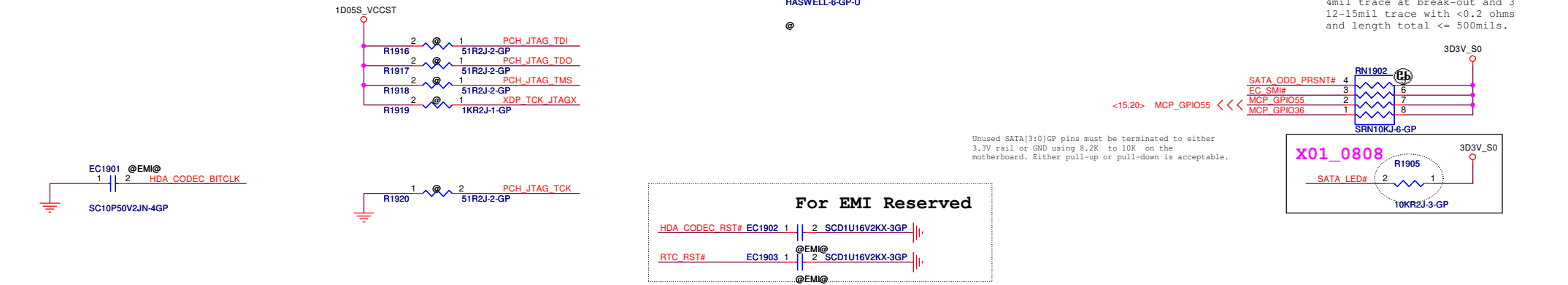
Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs★



PCH strap pin:

Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default ★ High = Enable

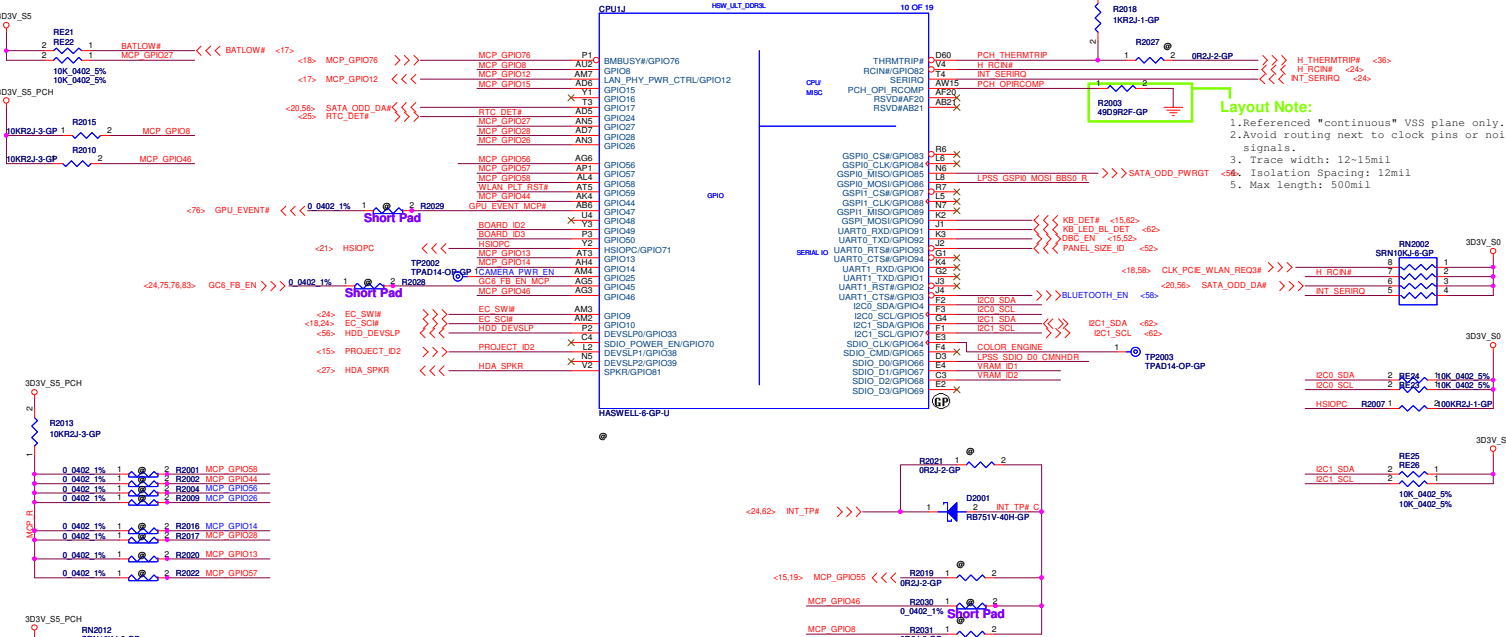
The internal pull-down is disabled after PLTRST# deasserts



For EMI Reserved			
HDA CODEC RST#	EC1902	1	2
RTC RST#	EC1903	1	2

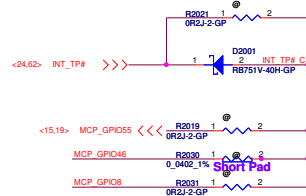
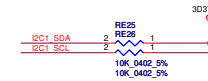
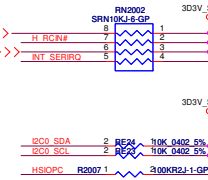
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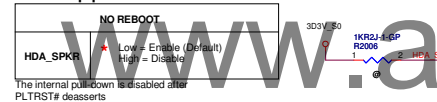


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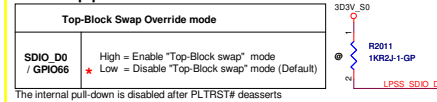
1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil



PCH strap pin:

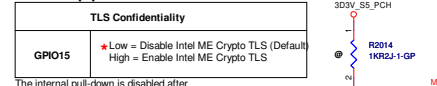


PCH strap pin:



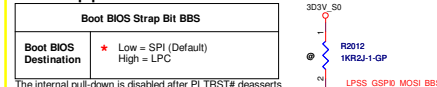
Need SW double confirm if that's needed Top-Block swap

PCH strap pin:



The internal pull-down is disabled after RSMRST# deasserts.

PCH strap pin:



Need double confirm, GPIO table set to GPI if that's needed PH or PL

BIOS strap pin:

BIOS UMA/DIS Strap pin	BOARD_ID2
UMA	0
DIS	1

BIOS strap pin:

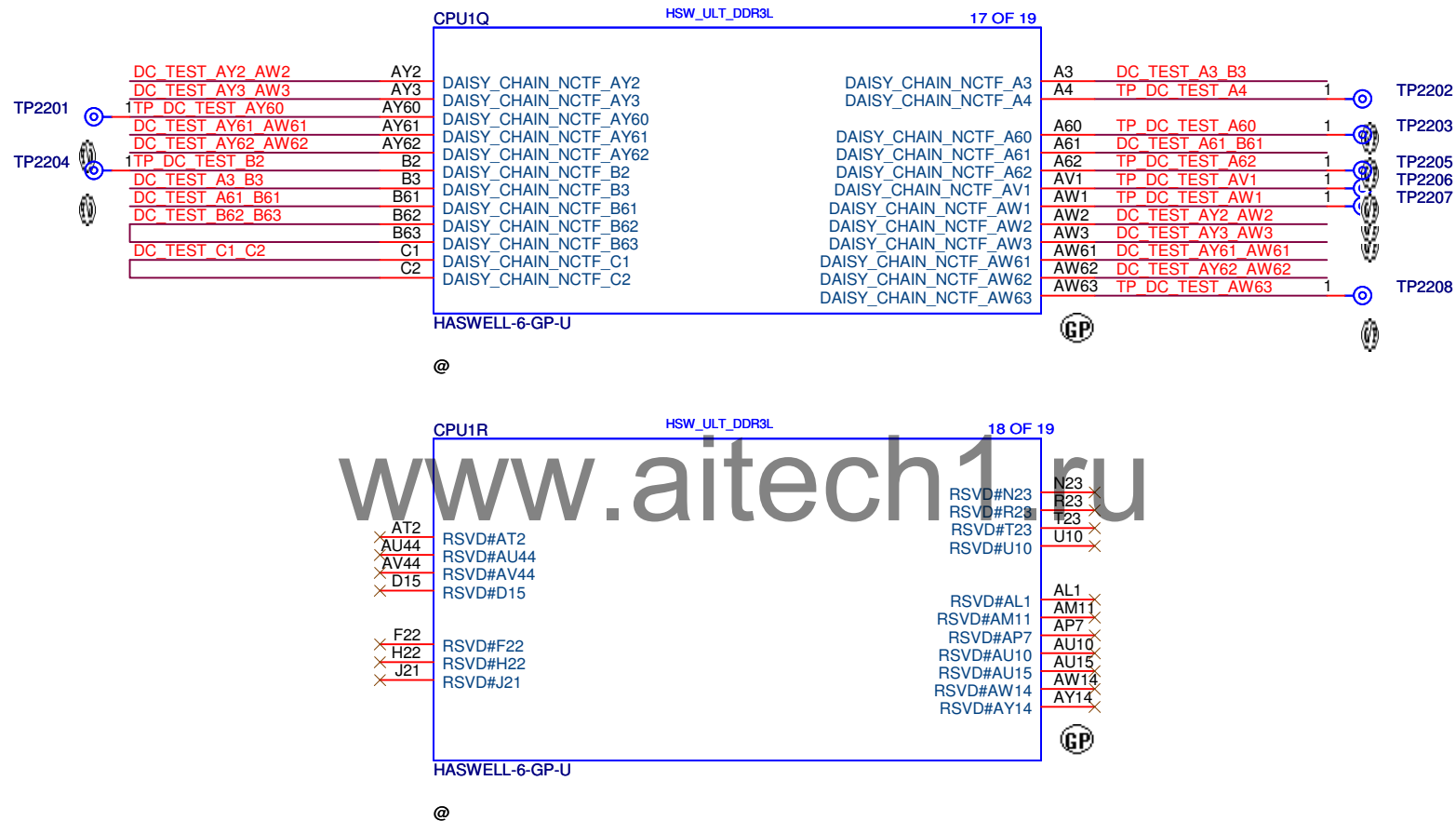
BIOS UMA/DIS Strap pin	BOARD_ID3
N15V-GM	0
N16V-GM	1

BIOS strap pin:

BIOS VRAM Size Strap pin	VRAM_ID2	VRAM_ID1
1G	0	0
2G	0	1
4G	1	0

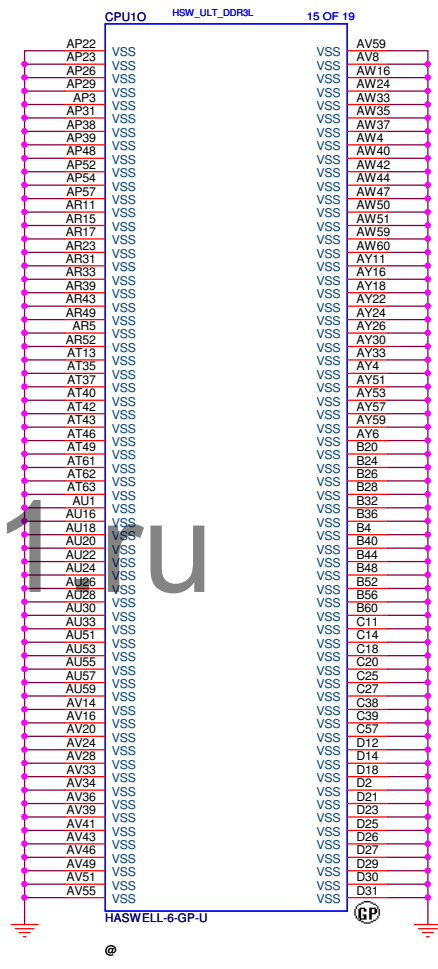
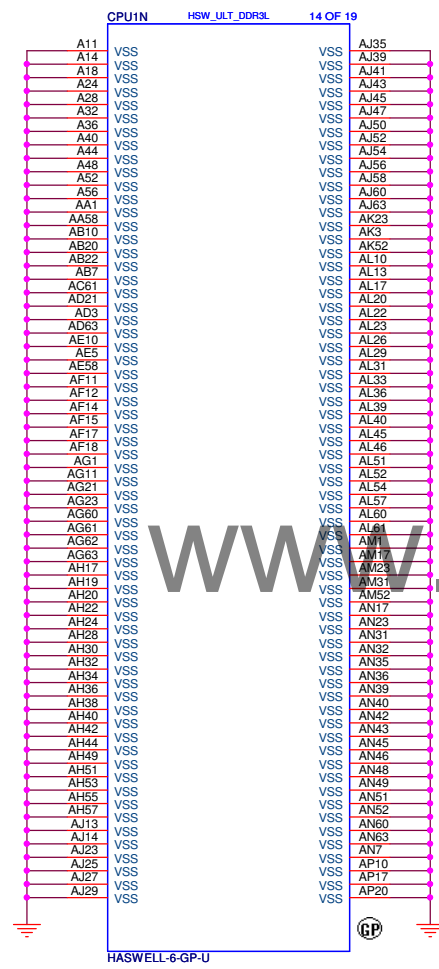
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Main Func = PCH



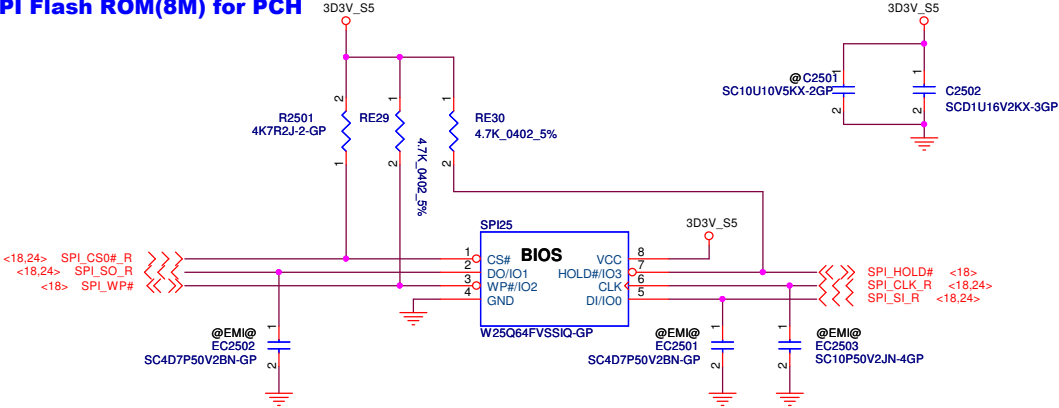
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Issued Date		2015/01/20		Deciphered Date		2015/12/31		Title	
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		Document Number		Rev					
		<i>LA-B483P</i>		A00					
Date:		Wednesday, January 21, 2015		Sheet		22		of 102	

Main Func = PCH

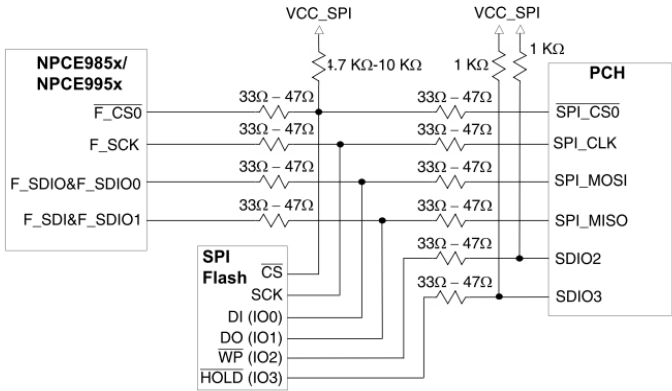


Main Func = SPI Flash

SPI Flash ROM(8M) for PCH



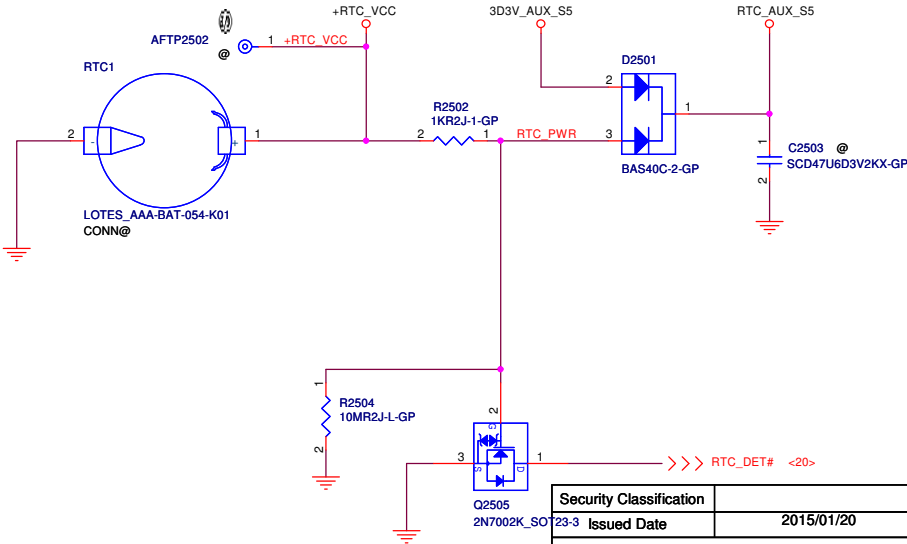
Single SPI shared flash connection (SPI Quad I/O mode)



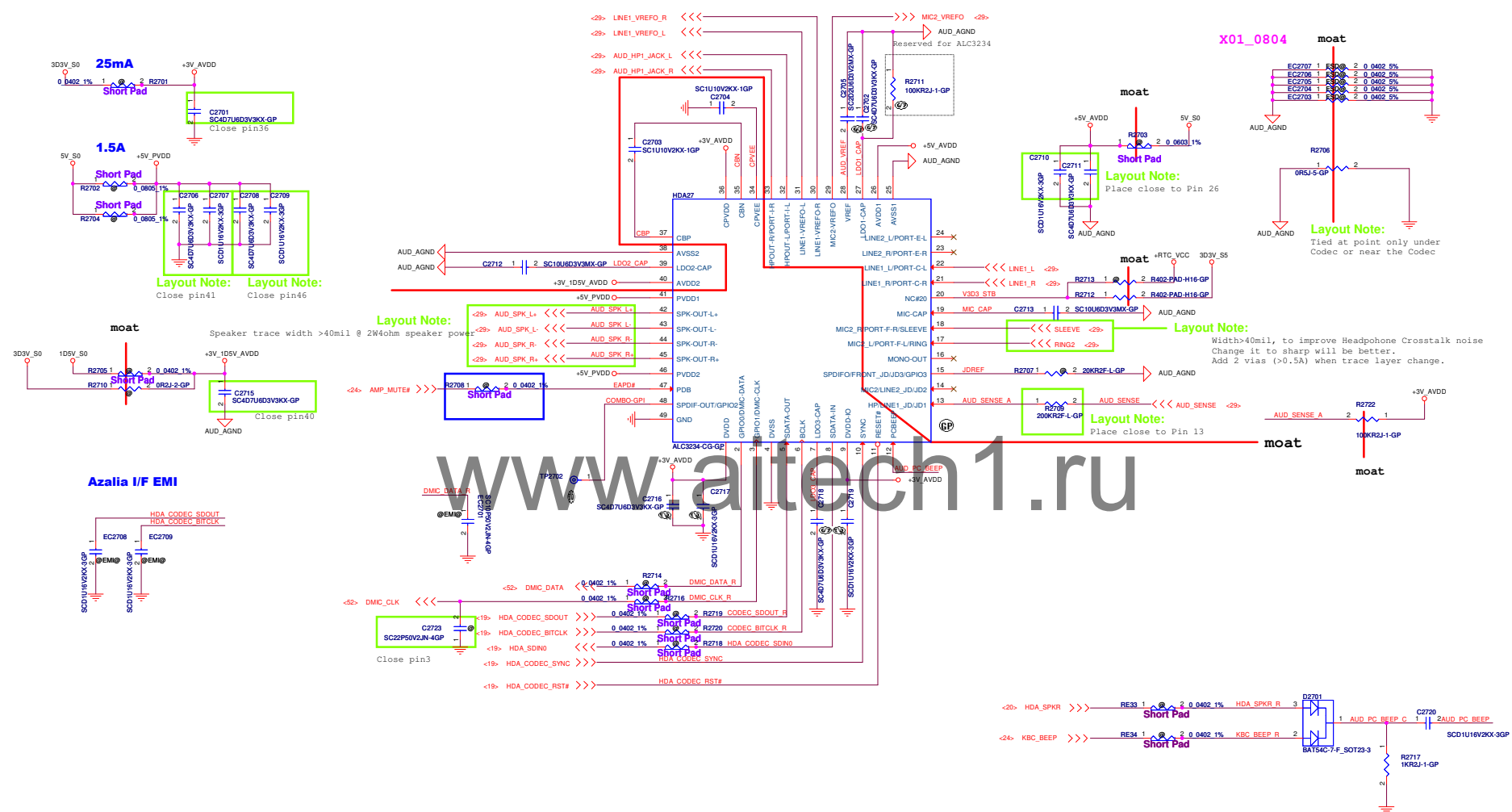
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	o	o
72.25647.00A	o	o
072.25B64.0001	o	o

Refer to "NPCE985x/ NPCE995x board design reference guide"

Main Func = RTC



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Date:				Wednesday, January 21, 2015				Sheet 25 of 102			
Rev				A00							



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Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title: Document Date: Yongjun Chen 21, 2015
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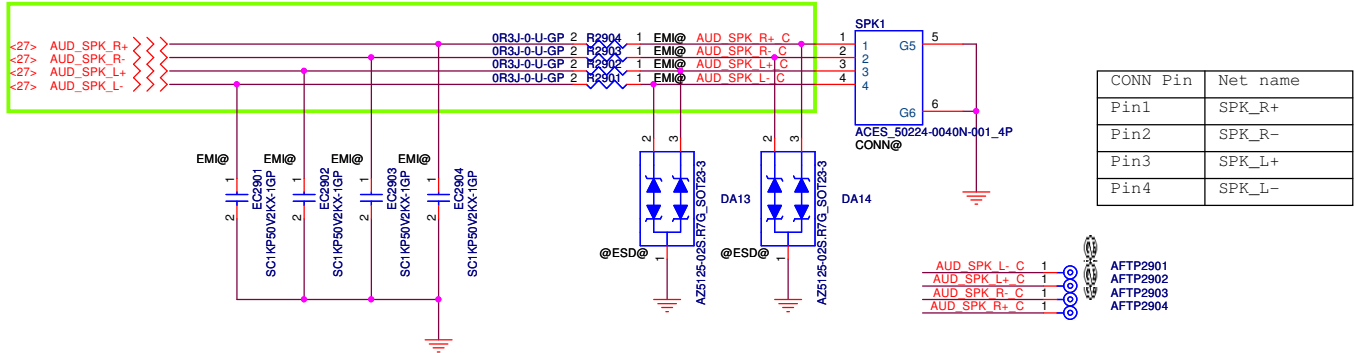
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title	
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				Document Number	Rev
				LA-B483P	A00
Date:		Wednesday, January 21, 2015		Sheet	28 of 102

Main Func = Audio

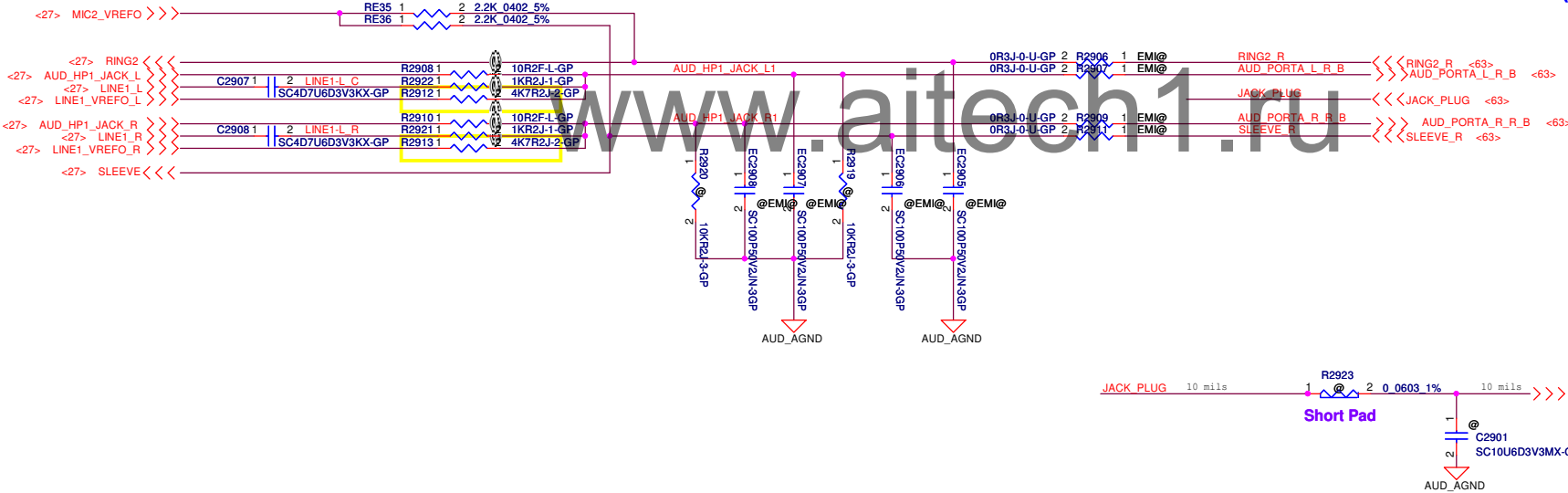
Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

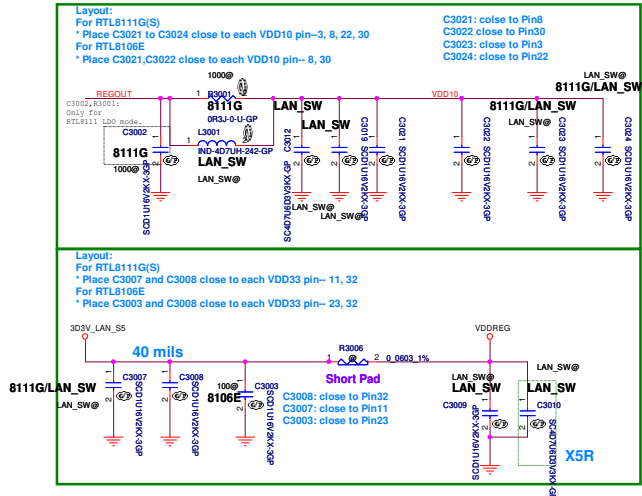
Speaker



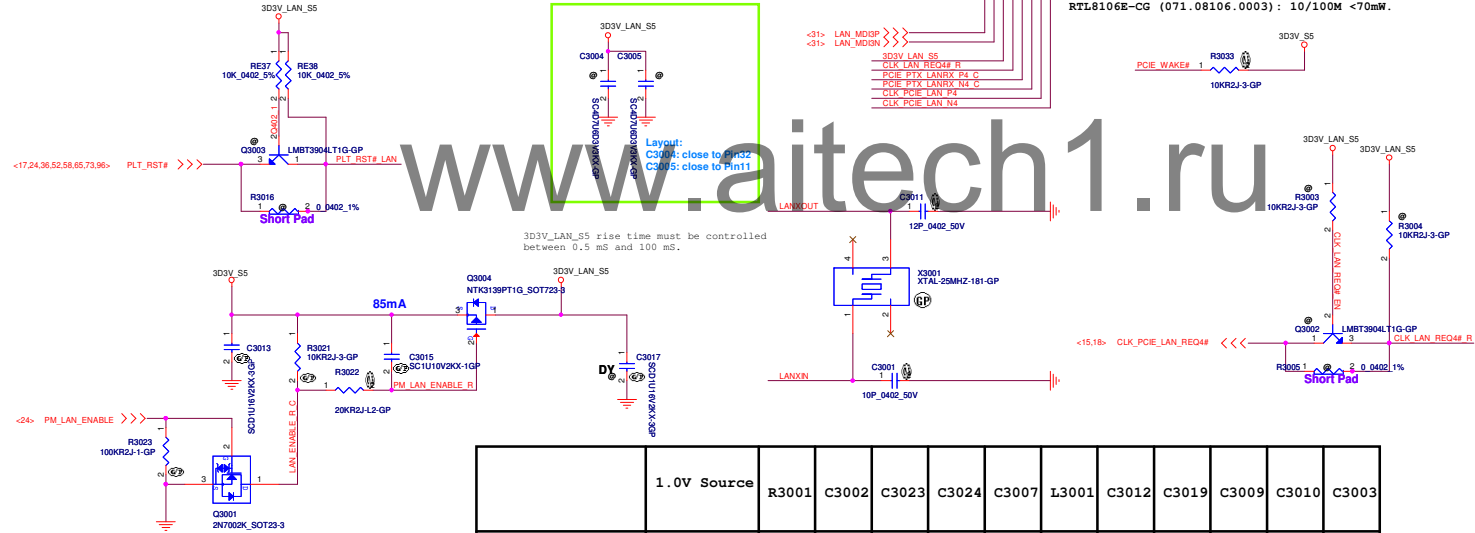
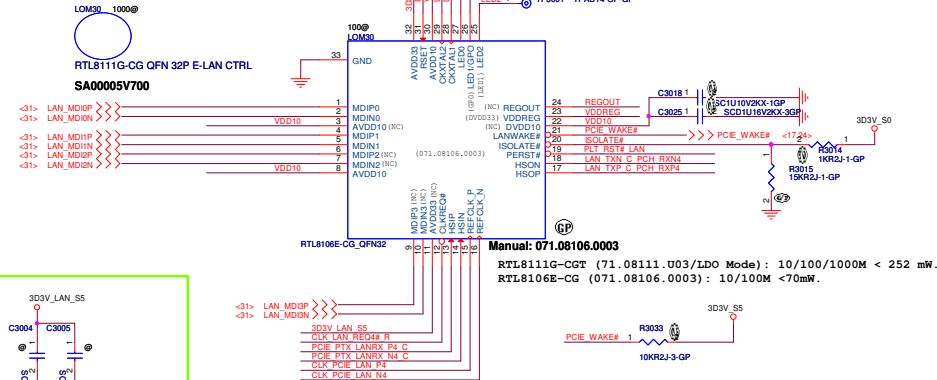
Universal Jack (Moved to I/O Board)



LAN CHIP (10/100/1000M & 10/100M co-lay)

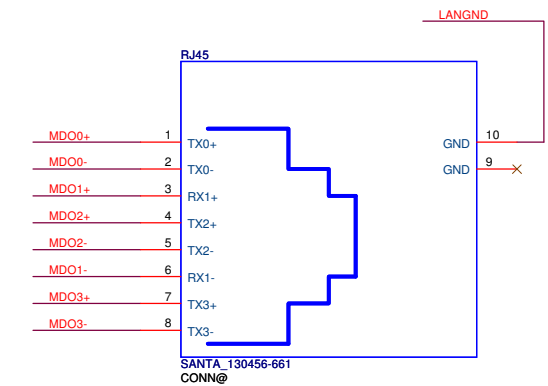
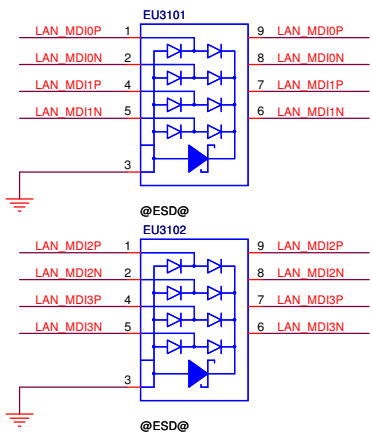
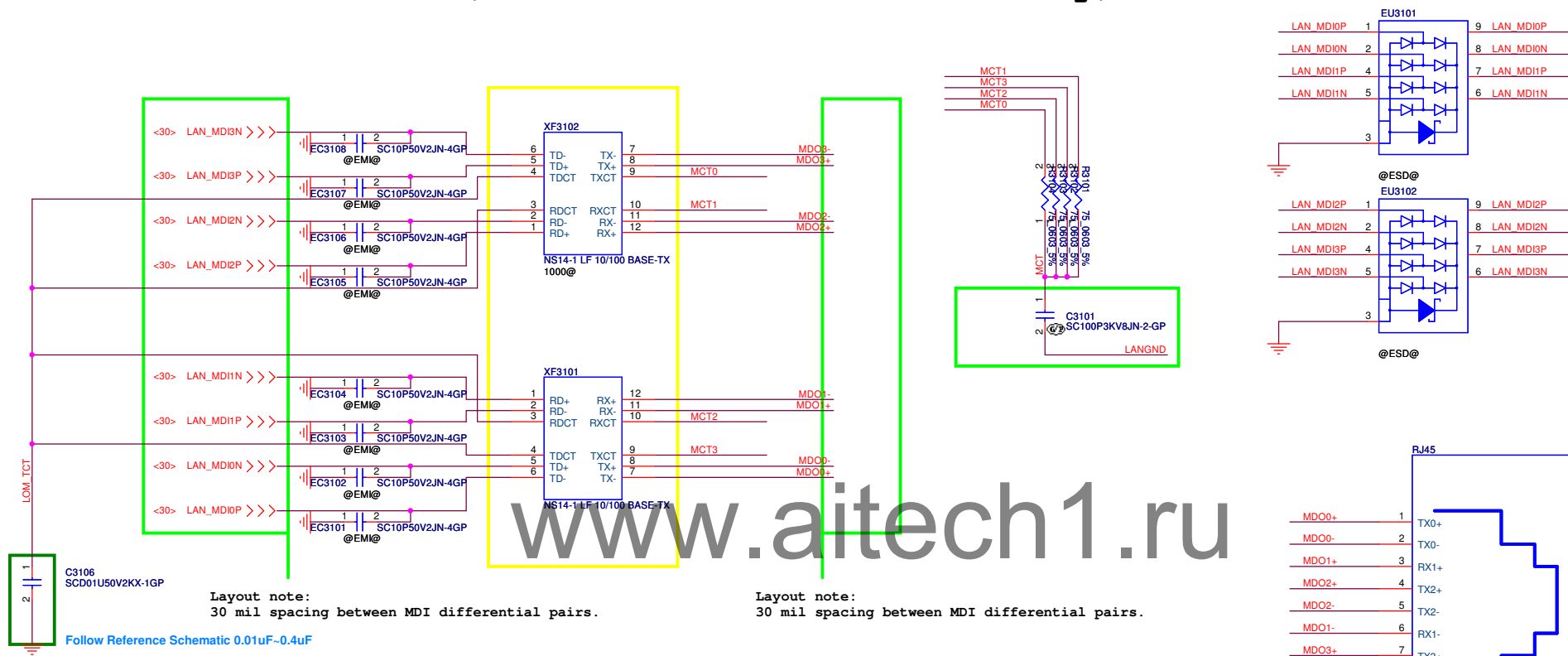


RTL8111GUS-CG	RTL8111G-CGT	RTL8106EUS-CG	RTL8106E-CGT
71.08111.W03	71.08111.W03	71.08106.W03	071.08106.0003
SWR mode	LDO mode	SWR mode	LDO mode
10/100/1000M	10/100/1000M	10/100M	10/100M

[illegible]

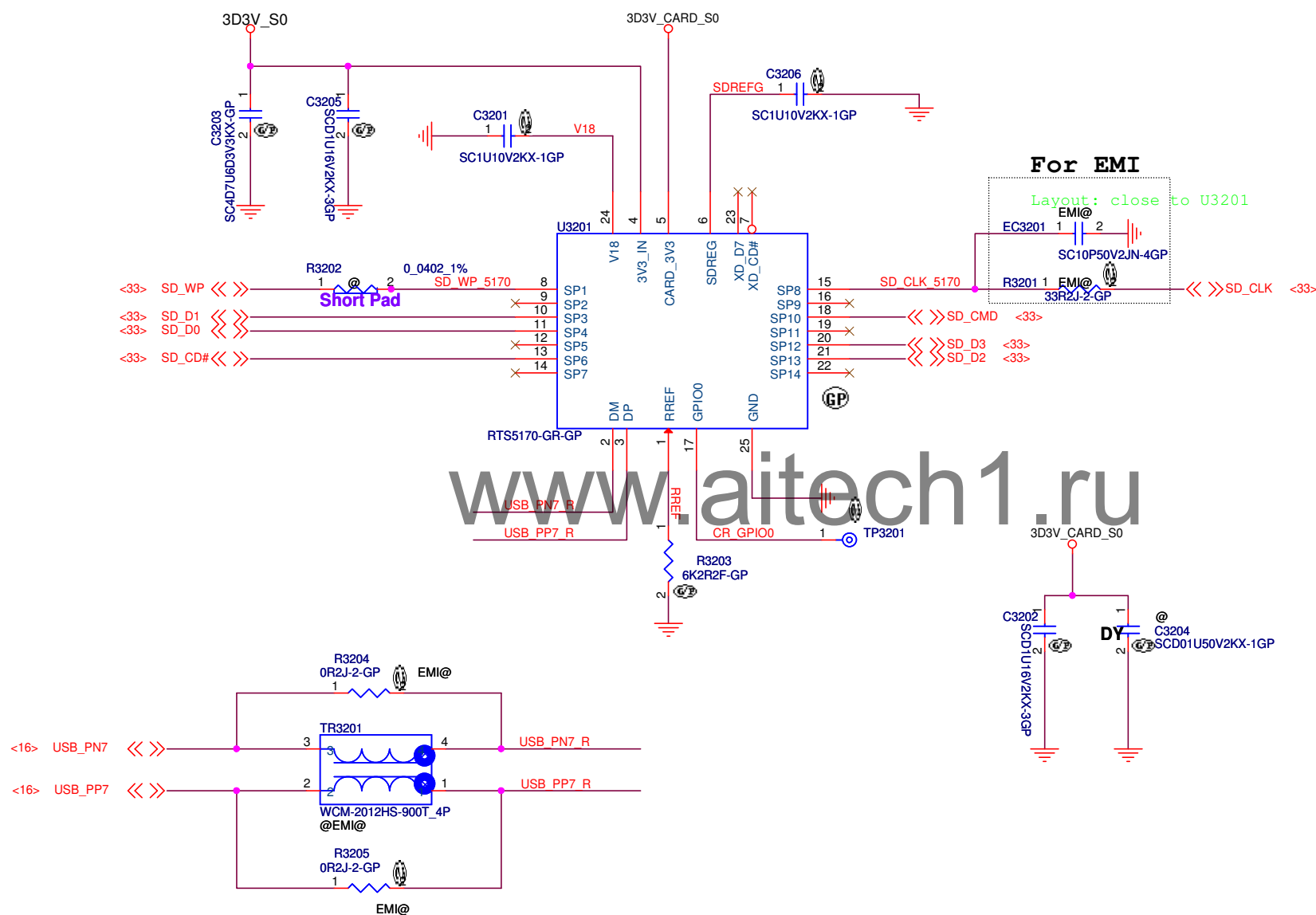
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Issued Date	2015/01/20	Deciphered Date	2015/12/31	
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Date:			Wednesday, January 21, 2015	Sheet 30 of 102

LAN TransFormer (10/100/1000M & 10/100M co-lay)



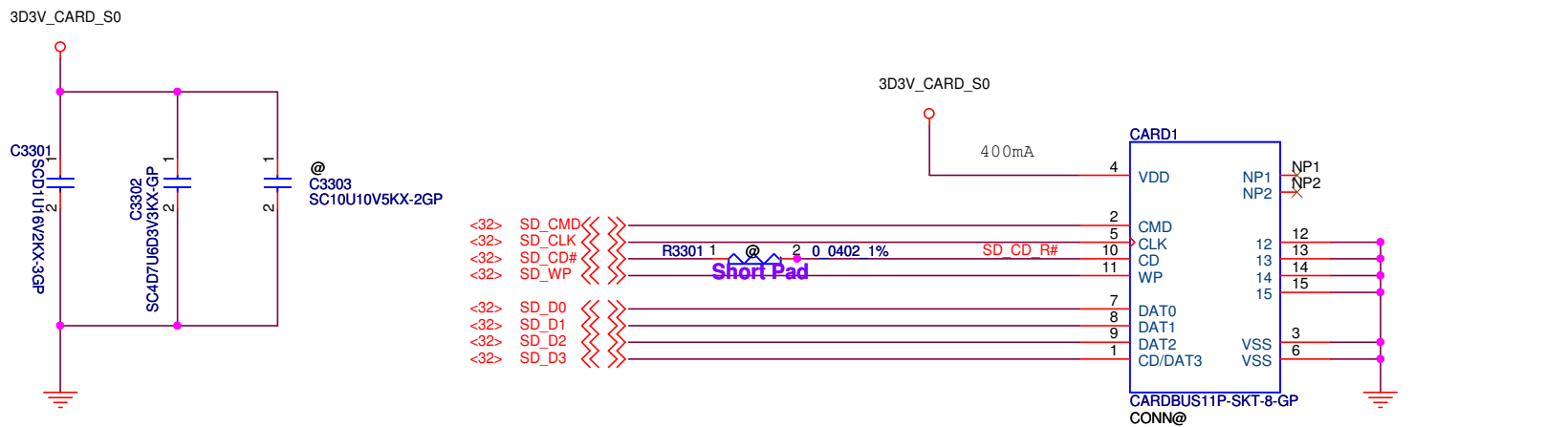
Main Func = Card Reader

The maximum range of the PMOS output current in RTS5170 (Card Reader IC) is 400mA

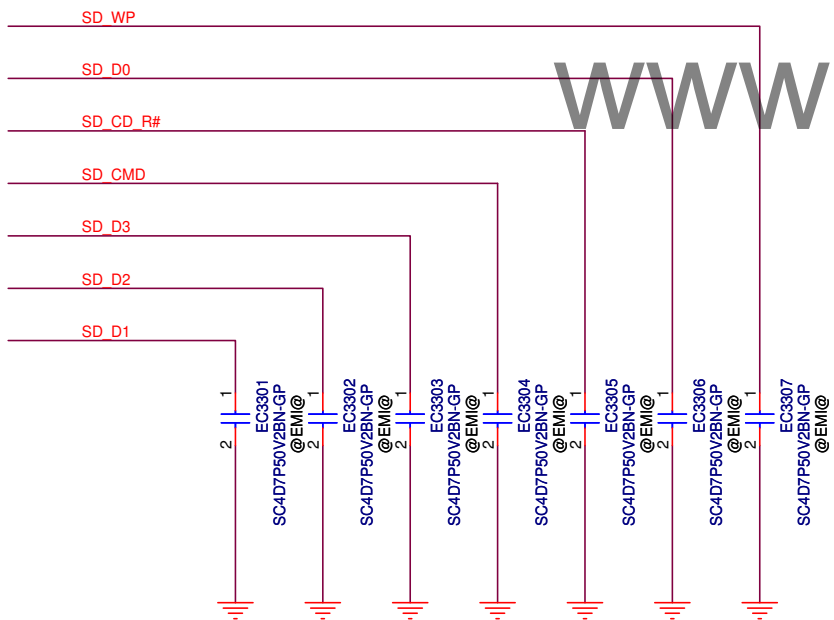


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				Size	Document Number	Rev A0
				LA-B483P		
Date: Wednesday, January 21, 2015				Sheet	32	of 102

Main Func = Card Reader



For EMI Reserved

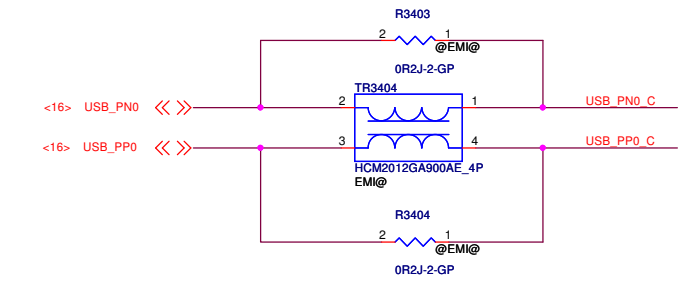


SD CMD	1	○	AFTP3302
SD CLK	1	○	AFTP3303
SD CD R#	1	○	TP3304
SD WP	1	○	TP3305
SD D0	1	○	AFTP3306
SD D1	1	○	TP3307
SD D2	1	○	TP3308
SD D3	1	○	TP3309
3D3V CARD S0	1	○	TP3310

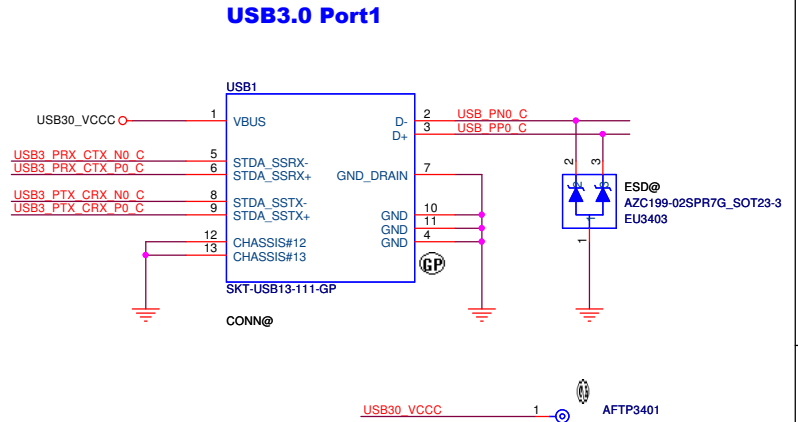
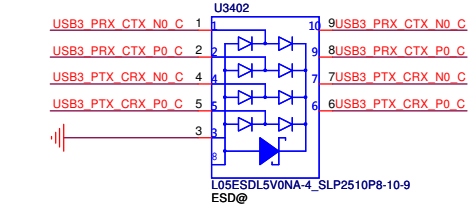
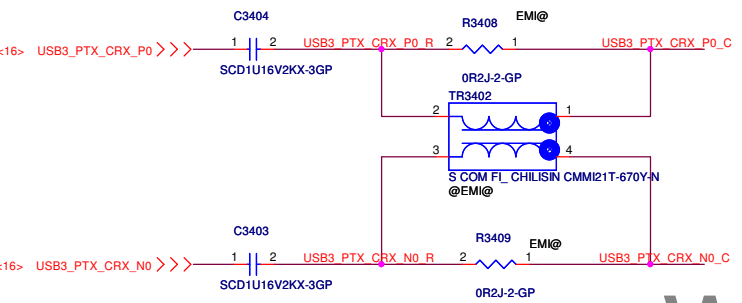
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Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title Card Reader-RTS5170		
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Date: Wednesday, January 21, 2015				Sheet	33	of 102

Main Func = USB3.0 Port1

USB2.0 Port2 and USB2.0 Port3 are on IOBD

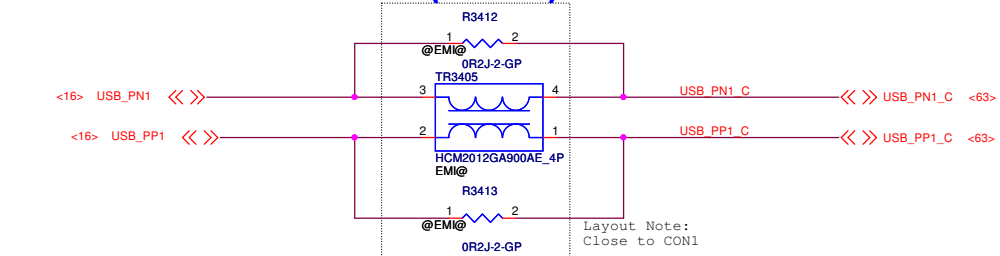


USB2.0/3.0 filter use SM070003Q00

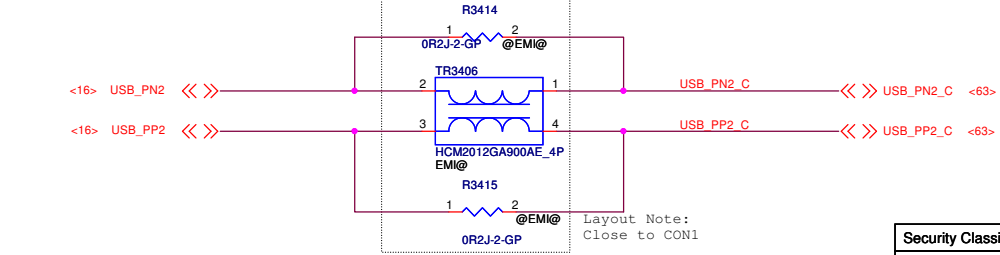


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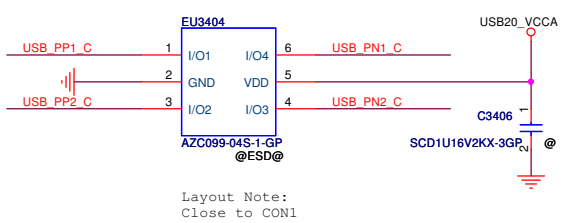
USB2 (USB2.0) CMC



USB3 (USB2.0) CMC

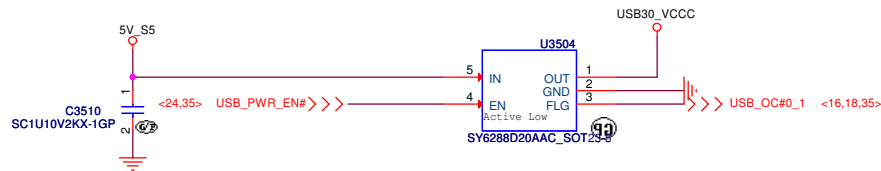


USB ESD Diode



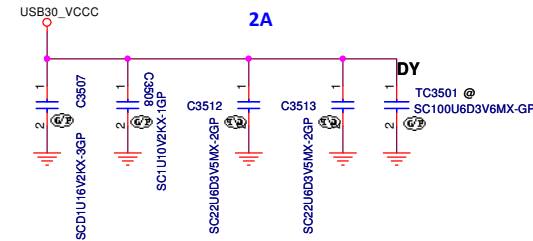
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Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title	USB3.0 CONN
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					LA-B483P
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Main Func = USB3.0 Port1



USB3.0 Port1

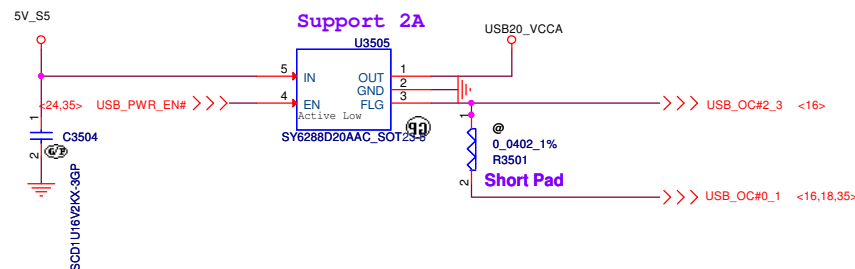
Layout Note: Close USB1



Main Func = USB2.0 Port2

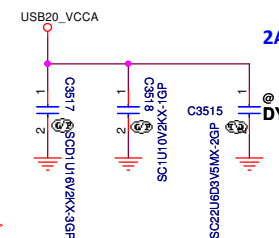
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Main Func = USB2.0 Port3



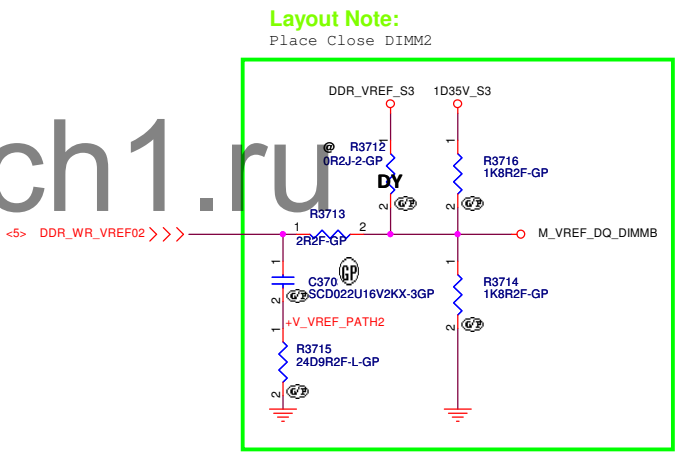
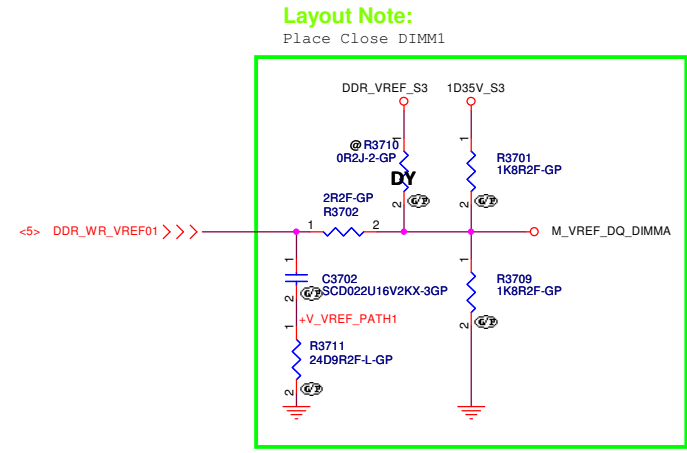
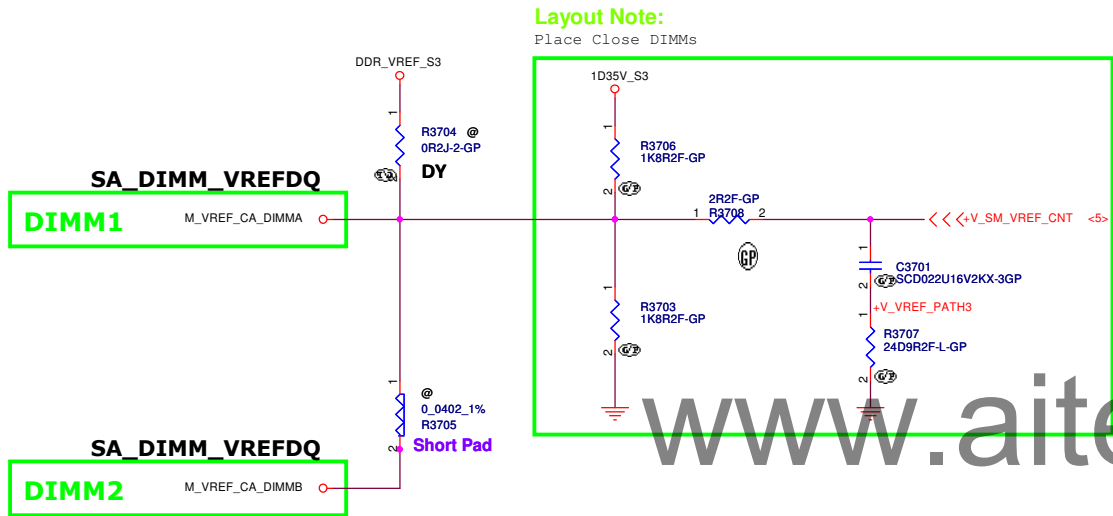
USB2.0 Port3 (IO Board)

Layout Note: Close CON1



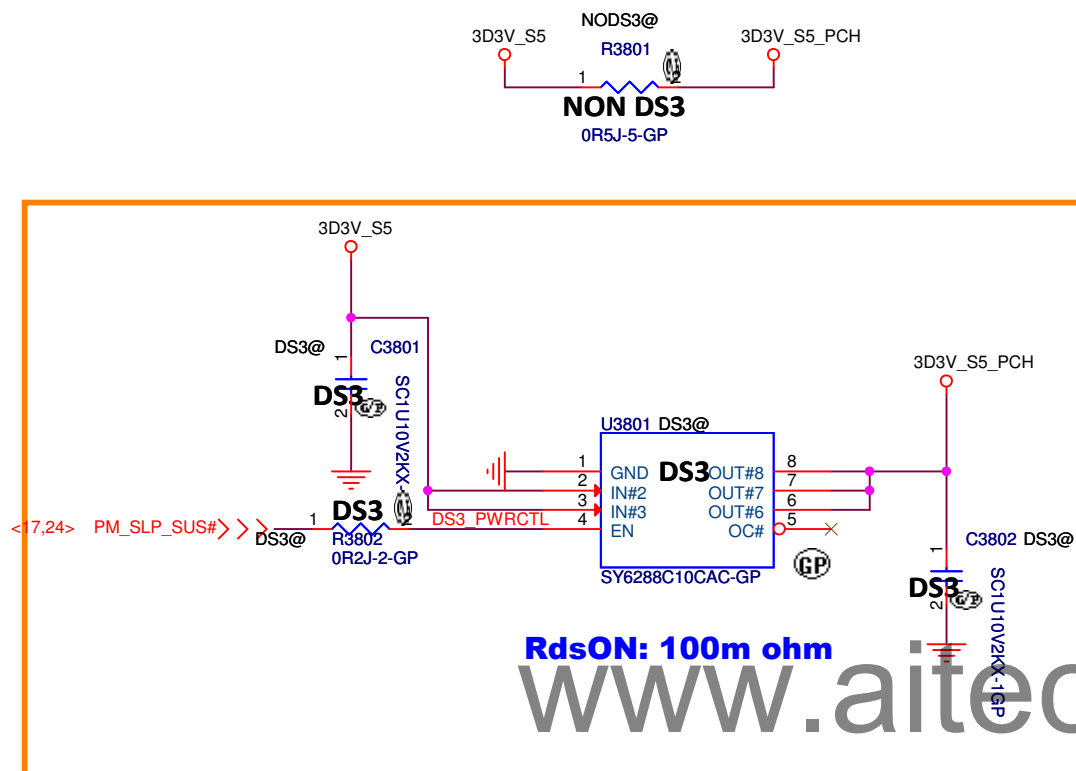
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Main Func = DIMM1
Main Func = DIMM2





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Main Func = Power Plane & Sequence



DS3

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				<div> <div>  </div> <div> Rev </div> </div>		
				<div> <div> Date: </div> <div> Wednesday, January 21, 2015 </div> </div> <div> <div> Sheet </div> <div> 38 </div> </div> <div> <div> of </div> <div> 102 </div> </div>		

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		Size		Document Number		Rev		A00	
		LA-B483P							
		Date:		Wednesday, January 21, 2015		Sheet 39 of 102			

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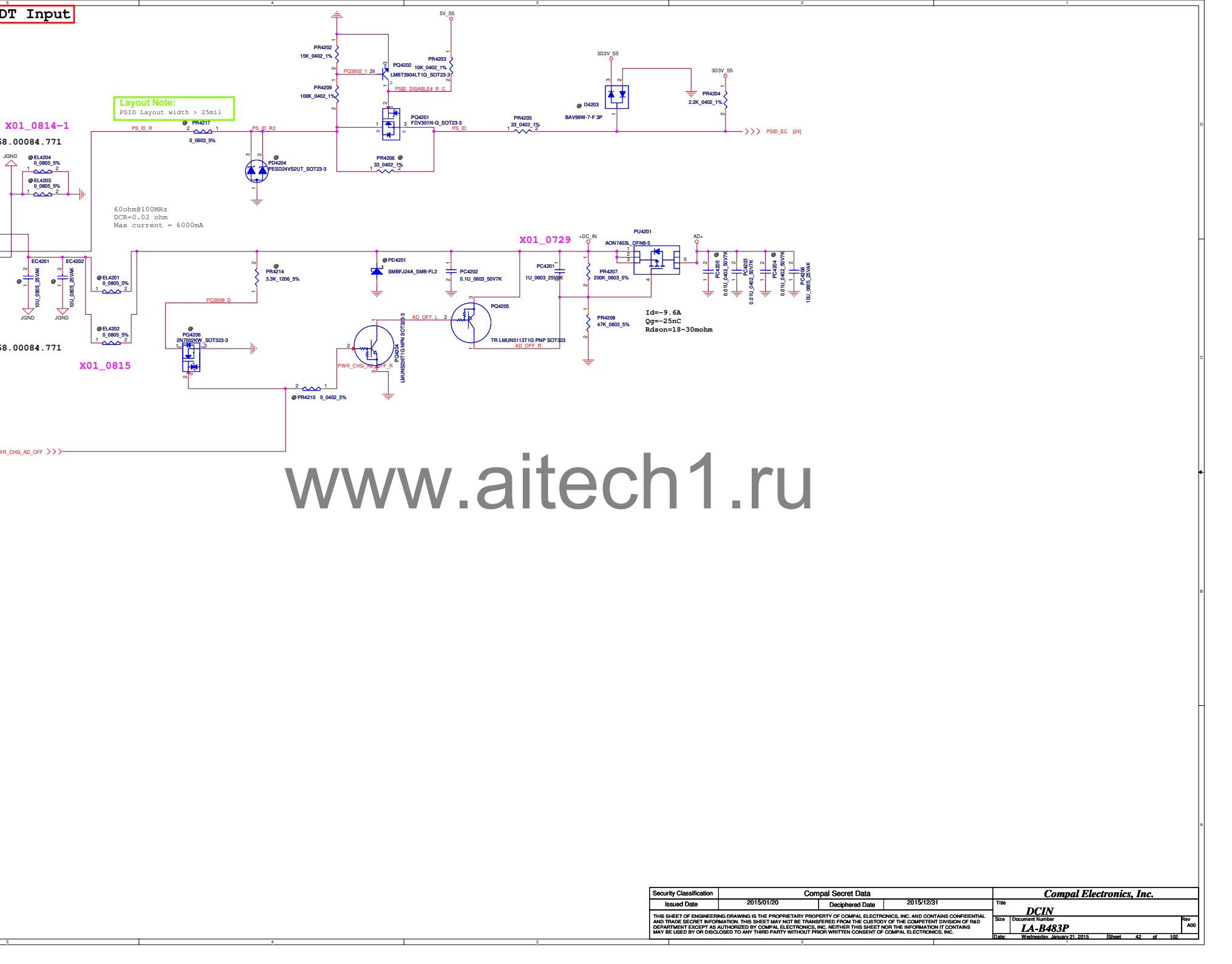
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					LA-B483P	A00
				Date:	Wednesday, January 21, 2015	Sheet 40 of 102

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						Date: Wednesday, January 21, 2015		Sheet 41 of 102	

[illegible]

DT Input

5V_S5

30V_S5

Layout Note:
PSID Layout width > 25mil

X01_0814-1

8.00084.771

60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA

X01_0815

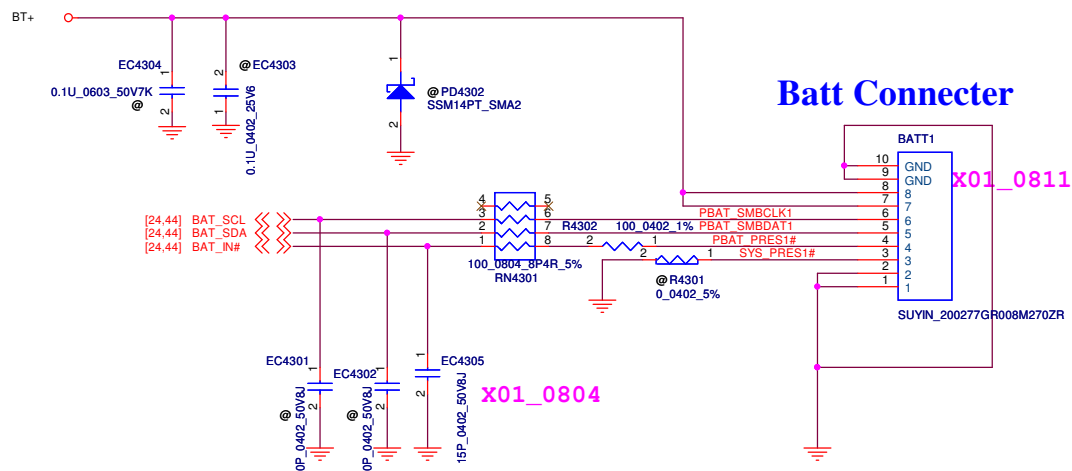
X01_0729

Id=-9.6A
Qg=-25nC
Rdson=18~30mohm

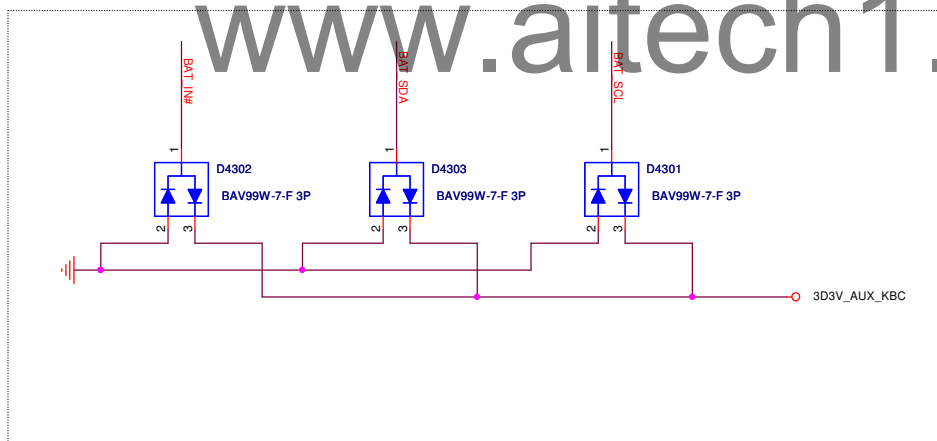
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Issued Date	2015/01/20	Deciphered Date	2015/12/31	DCIN
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Main Func = M-BAT Input

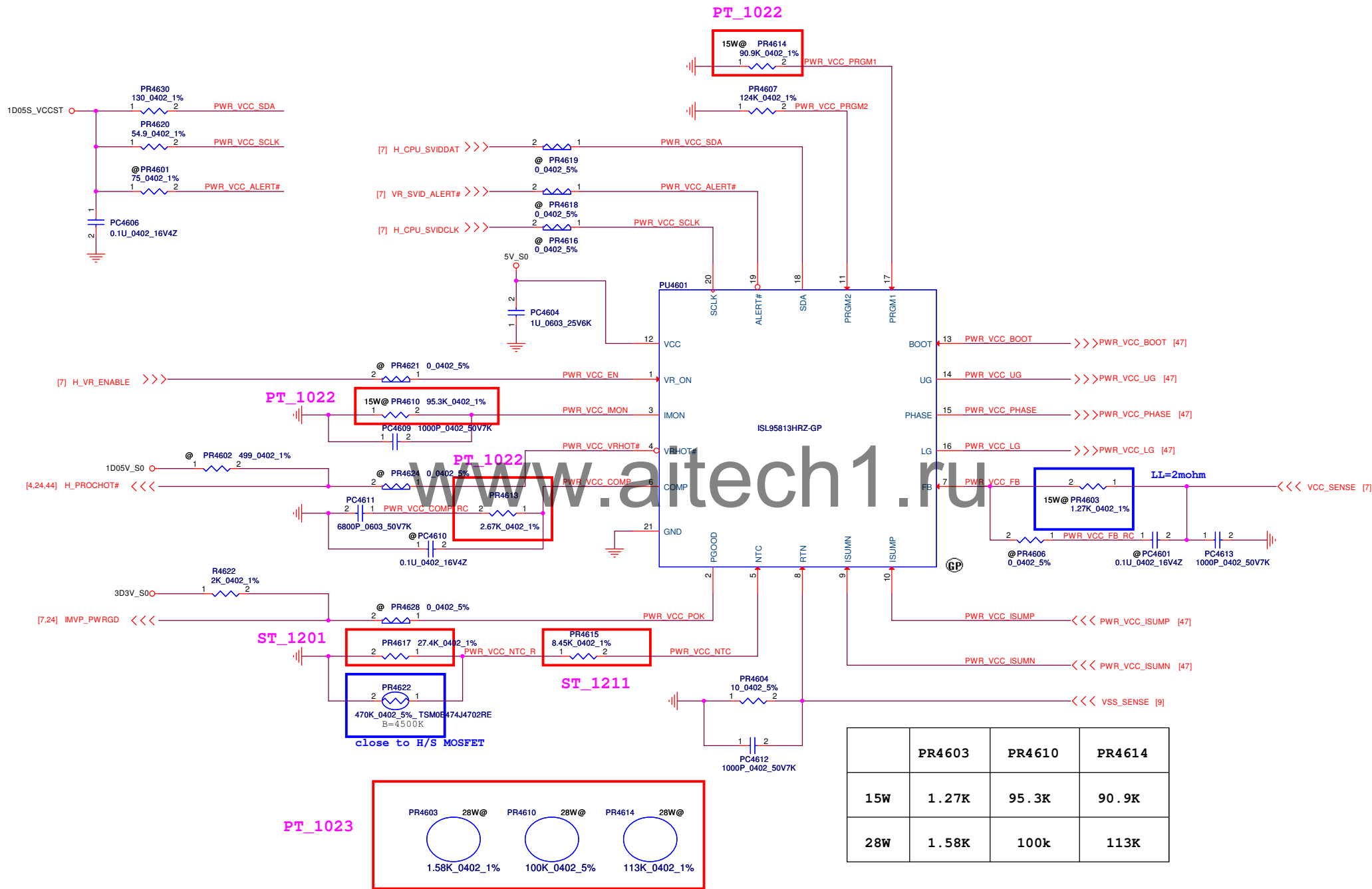


Placement: Close to Batt Connector



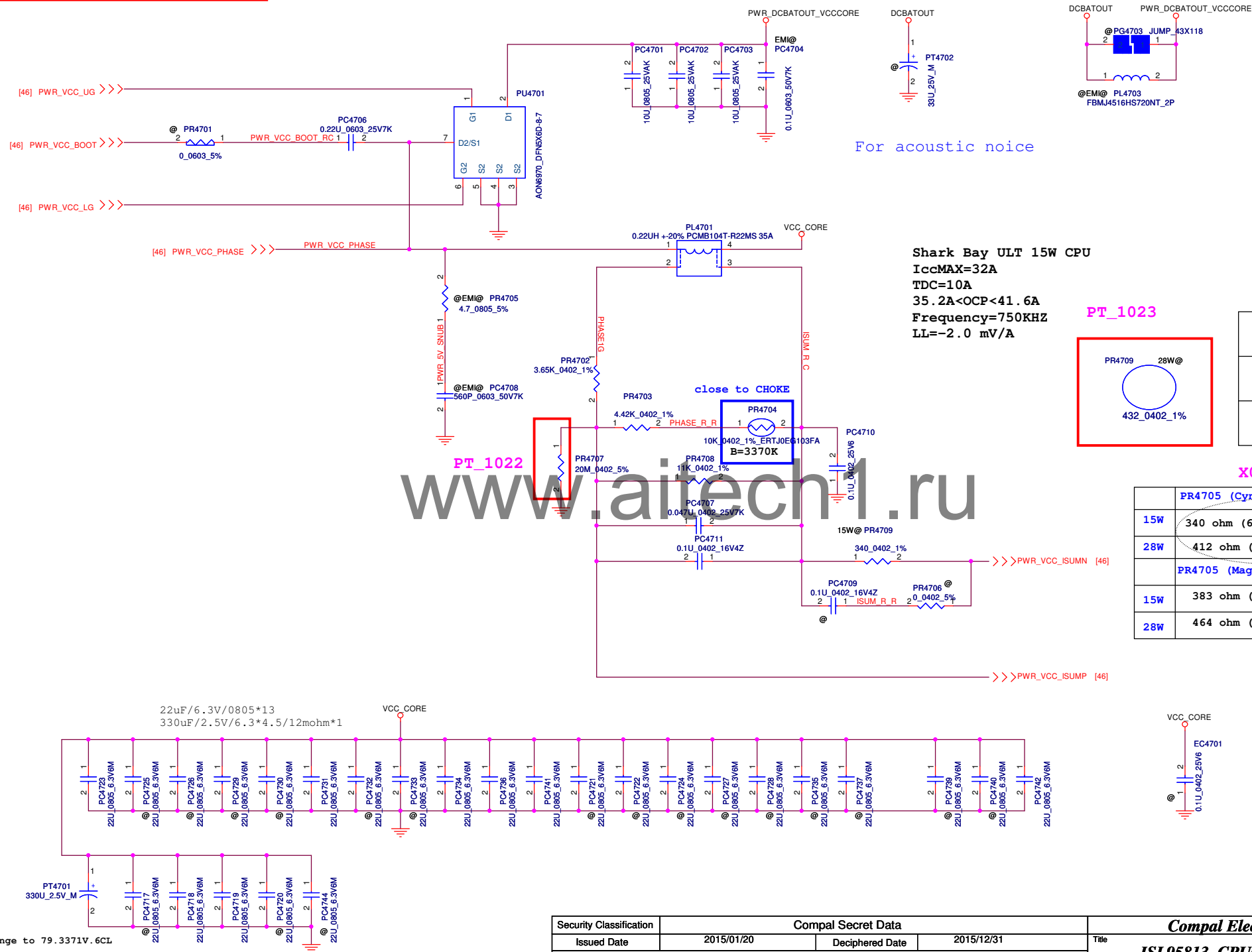
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title BATT CONN	
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Main Func = CPU_CORE



	PR4603	PR4610	PR4614
15W	1.27K	95.3K	90.9K
28W	1.58K	100k	113K

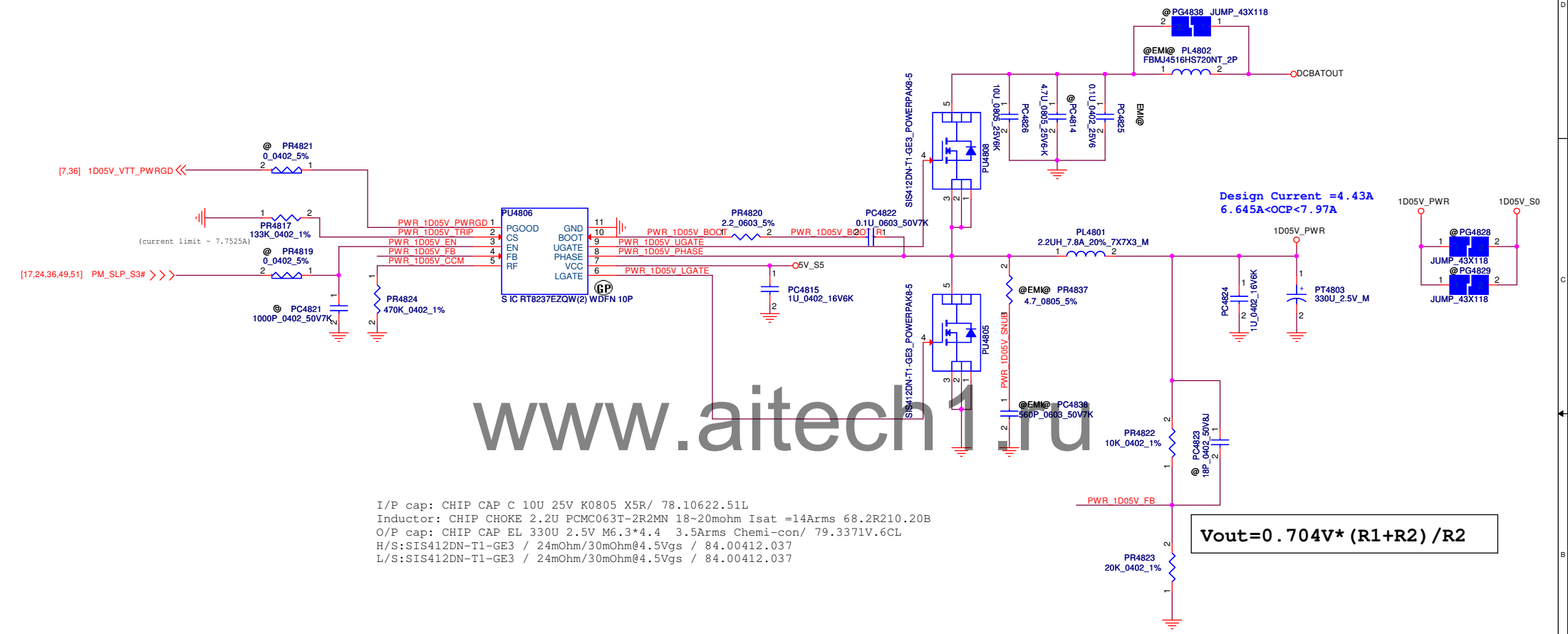
Main Func = CPU_CORE



	PR4709
15W	340 o-hm
28W	432 o-hm

	PR4705 (Cyntec choke)	OCF
15W	340 ohm (64.34005.6DL)	38A
28W	412 ohm (64.41205.6DL)	48A
	PR4705 (Maglayers choke)	
15W	383 ohm (64.38305.6DL)	38A
28W	464 ohm (64.46405.6DL)	48A

Main Func = 1D05V



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18~20mohm Isat =14Arms 68.2R210.20B
O/P cap: CHIP CAP EL 330U 2.5V M6.3*4.4 3.5Arms Chemi-con/ 79.3371V.6CL
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

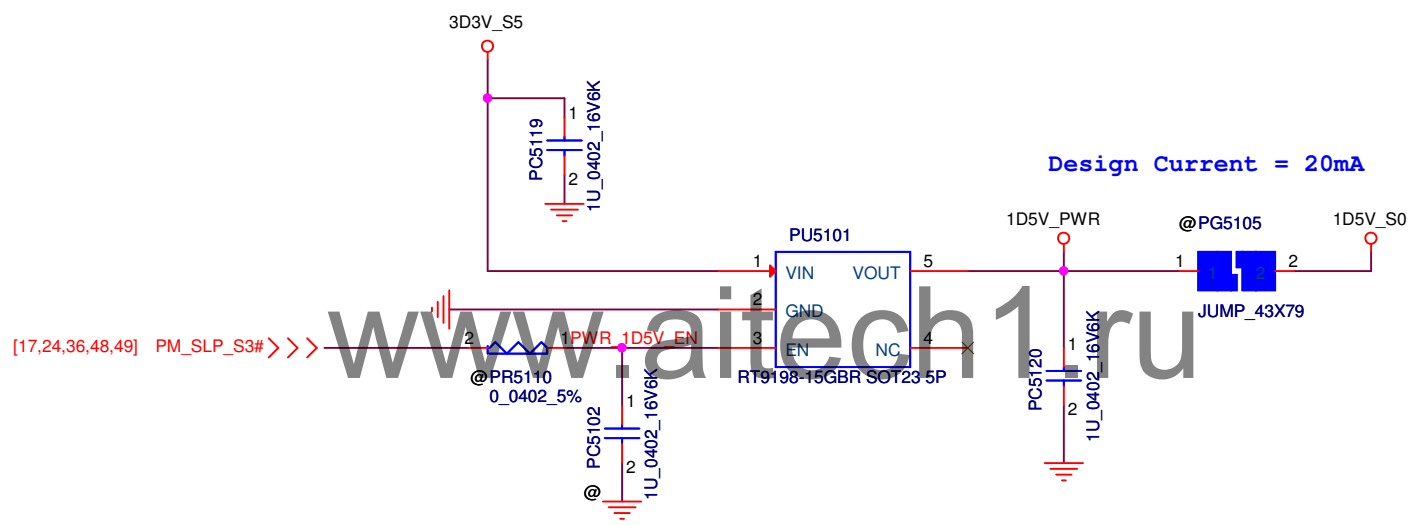
$$V_{out} = 0.704V * (R1 + R2) / R2$$

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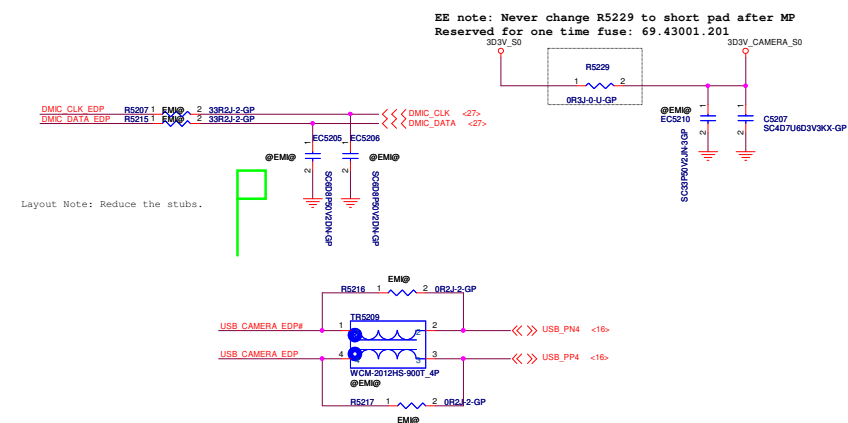
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Main Func = 1D5V

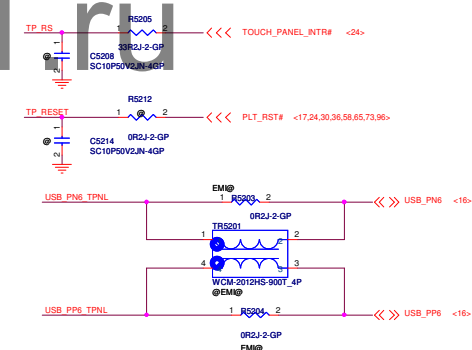


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Main Func = CAM



Touch Panel

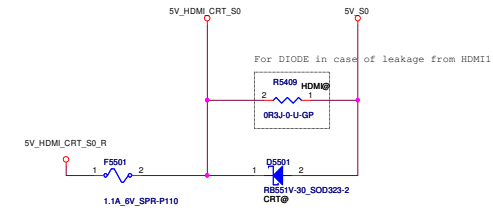
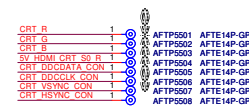
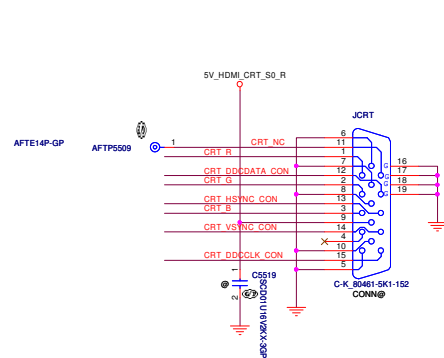


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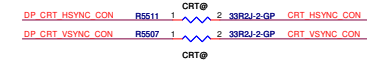
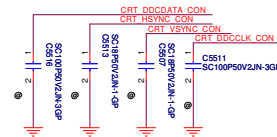
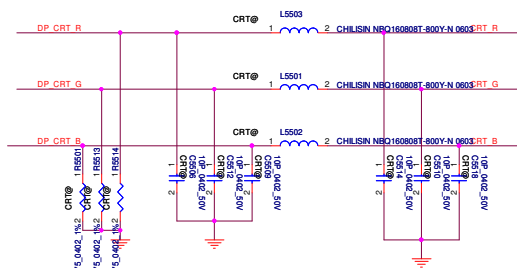
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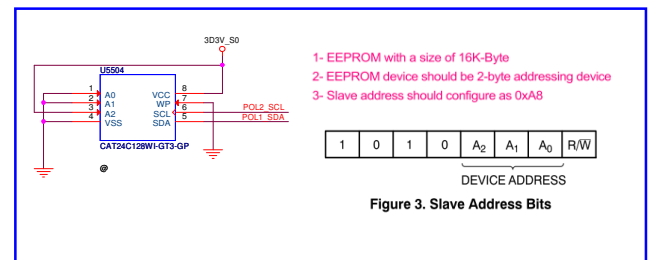
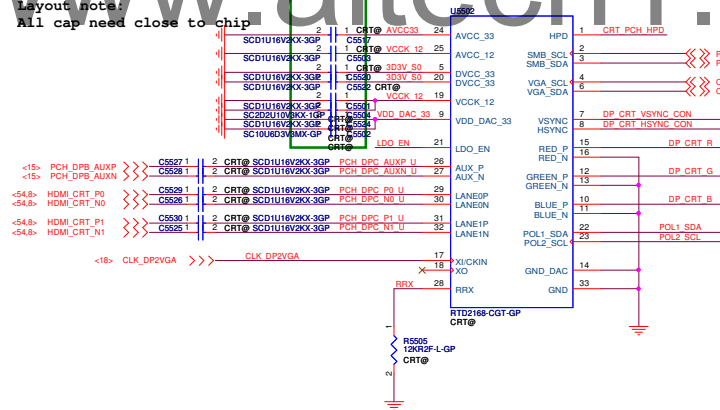
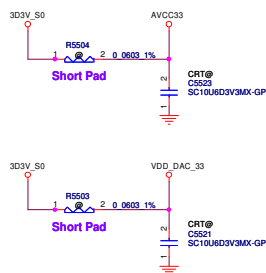
- 1- EEPROM with a size of 16K-Byte
- 2- EEPROM device should be 2-byte addressing device
- 3- Slave address should configure as 0xA8



CRT RGB
CRT H/VSYNC
CRT SMBUS



Layout note:
All cap need close to chip



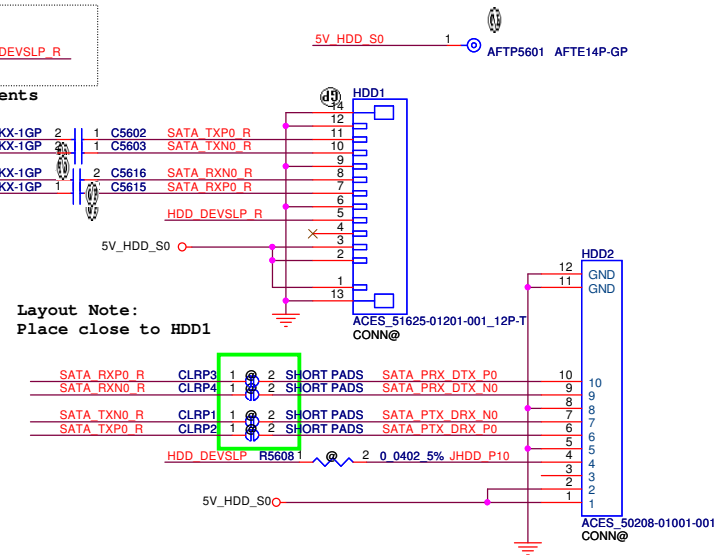
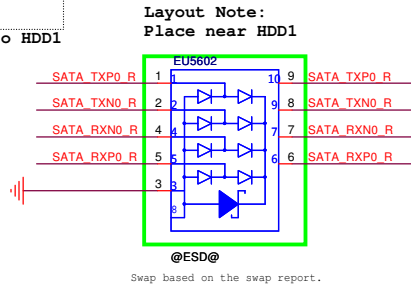
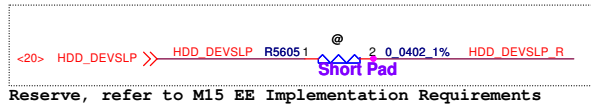
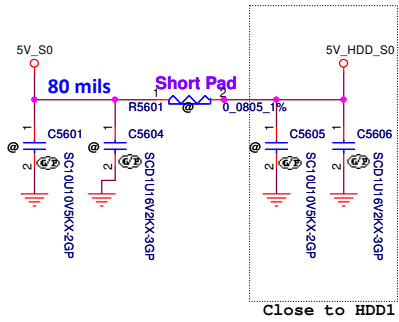
		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

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Main Func = HDD

SATA HDD Connector

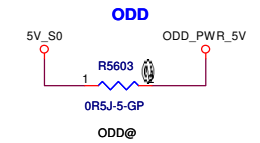
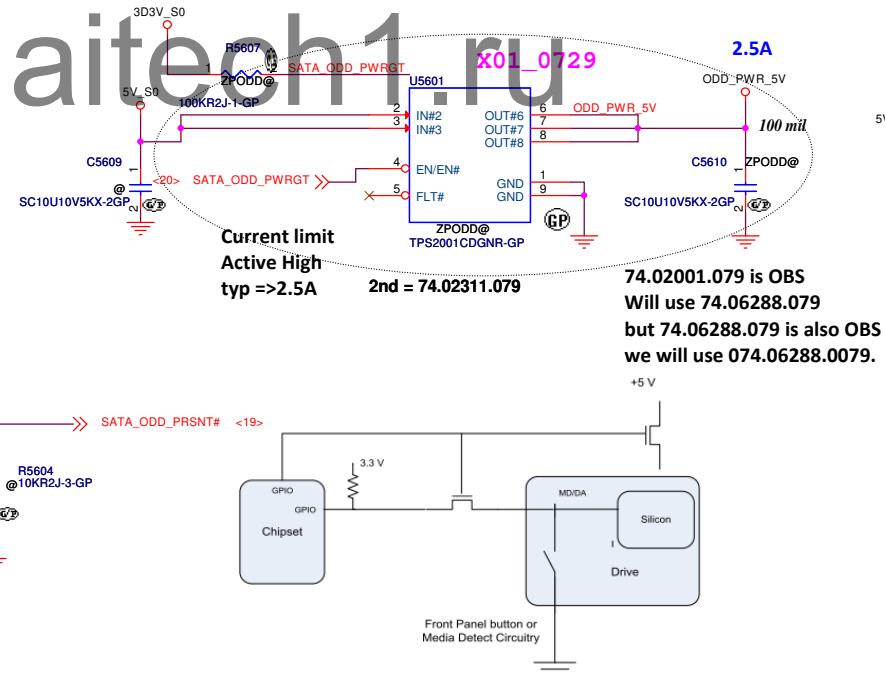
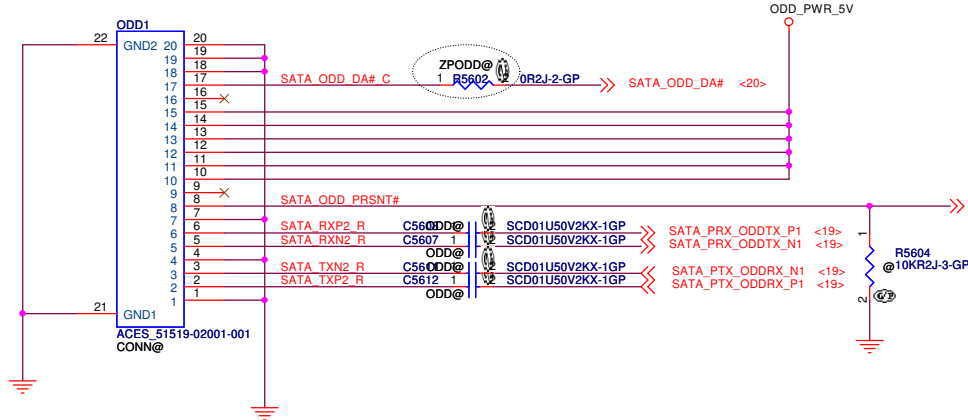


CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

Main Func = ODD

SATA Zero Power ODD

ODD Connector



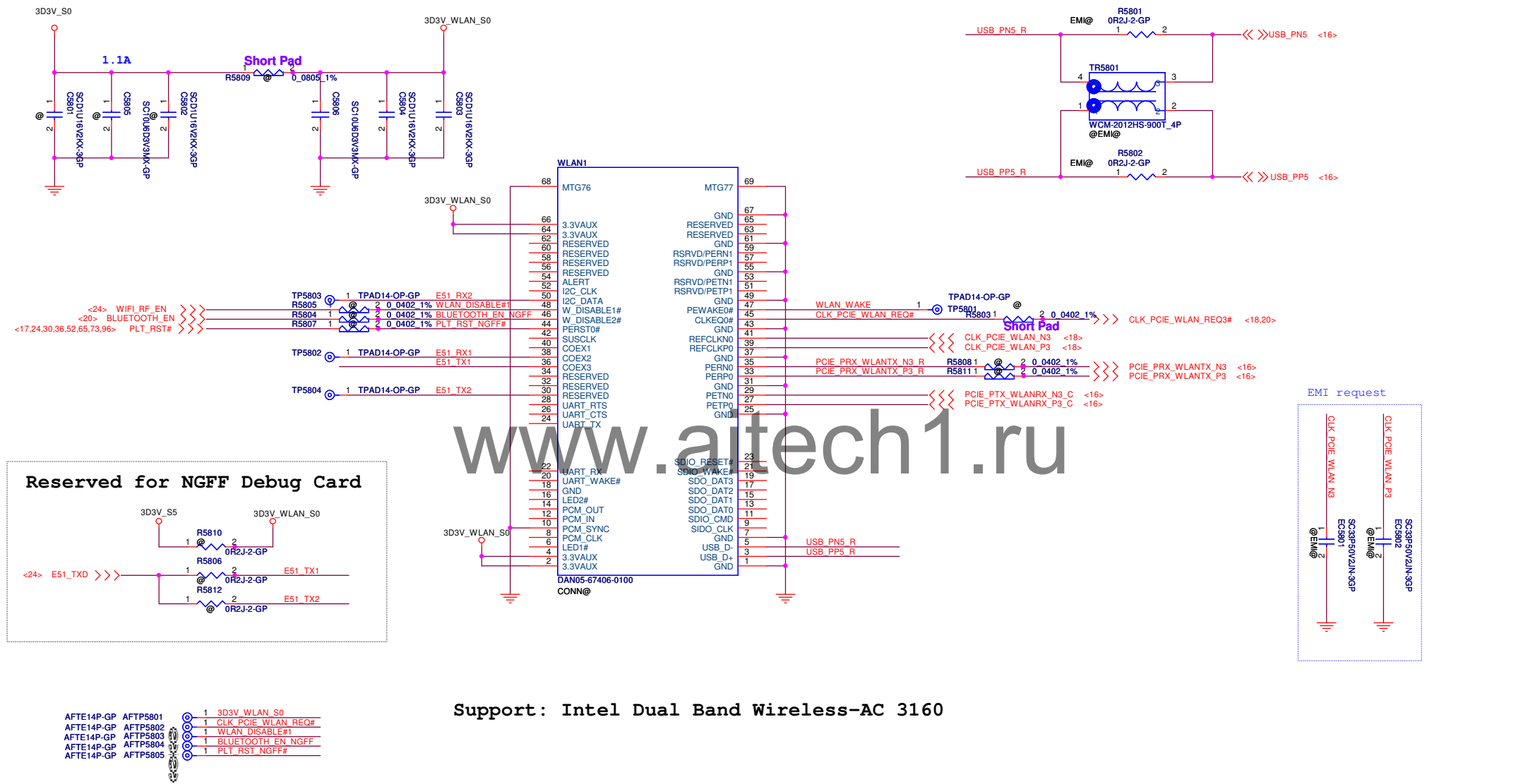
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SSID = ESATA

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Main Func = WLAN



Support: Intel Dual Band Wireless-AC 3160

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Main Func = IO Connector

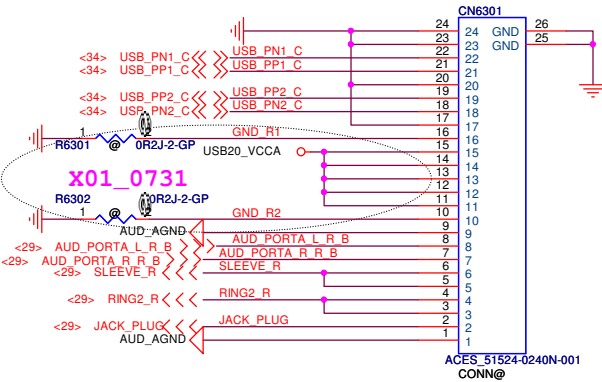
I/O Board Connector

X01_0808

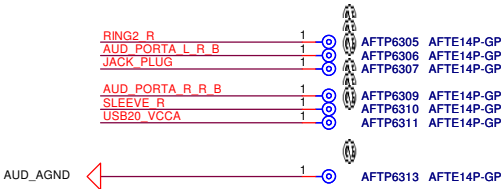
USB2 (USB2.0)
USB3 (USB2.0)

USB2 (USB2.0)
USB3 (USB2.0)

Universal Jack



Pitch: 1mm
Power: 5 pins
GND: 4 pins
AGND: 2 Pins



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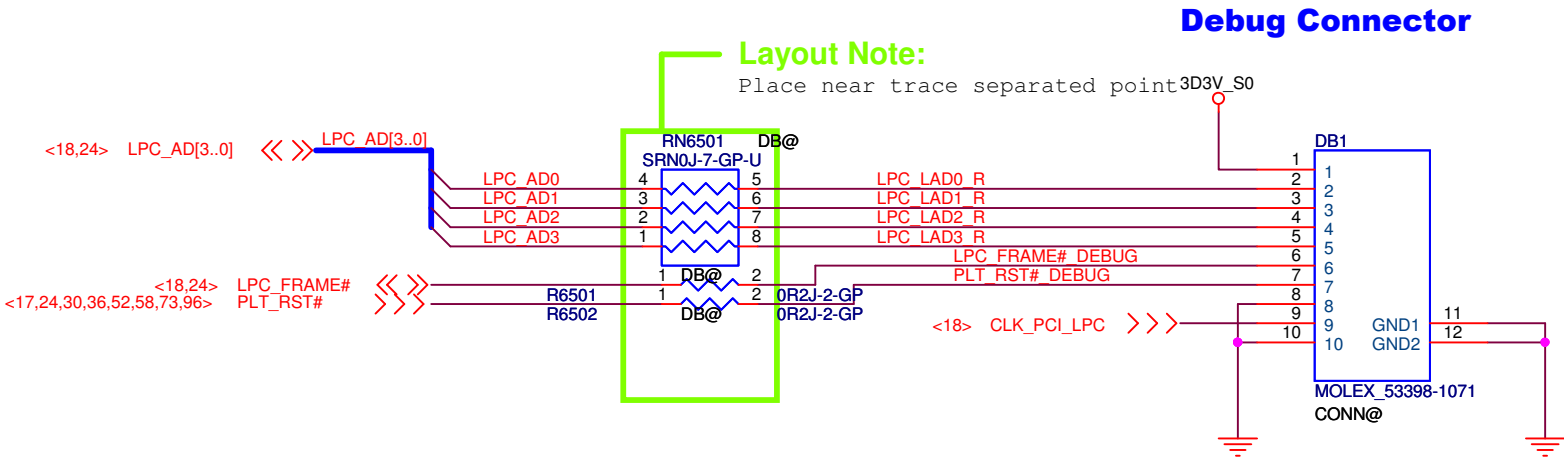
Main Func = Hall Sensor

Move to Power Button Board

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Main Func = Debug



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

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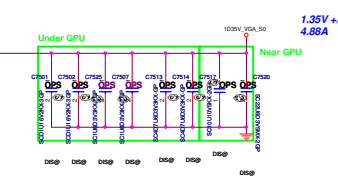
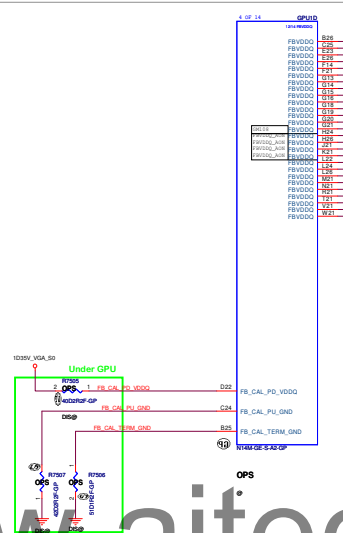
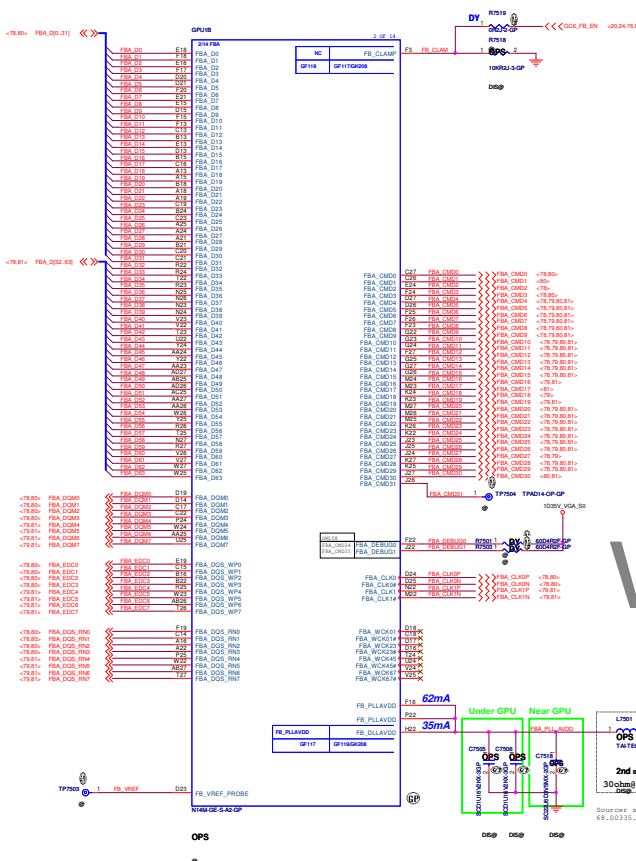
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Table 3-9. DDR3 GPU-side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2Z-64 DDR3	0.1 μ F	X7R 0402	2	Under GPU
	1 μ F	X7R 0603	2	Under GPU
	4.7 μ F	X6S 0603	2	Under GPU
	10 μ F	X5R 0805	1	Near GPU
	22 μ F	X5R 0805	1	Near GPU
GB4B-128 DDR3	0.1 μ F	X7R 0402	4	Under GPU
	1 μ F	X7R 0603	4	Under GPU
	4.7 μ F	X6S 0603	4	Under GPU
	10 μ F	X5R 0805	2	Near GPU
	22 μ F	X5R 0805	2	Near GPU

- Notes:**
1. The decoupling in this table applies to both single rank and dual rank designs.
 2. If a single partition 64-bit GPU in the GB4B-128 package is used, populate only half of the recommended number of decoupling capacitors of GB4B-128.



1.35V +
4.88A

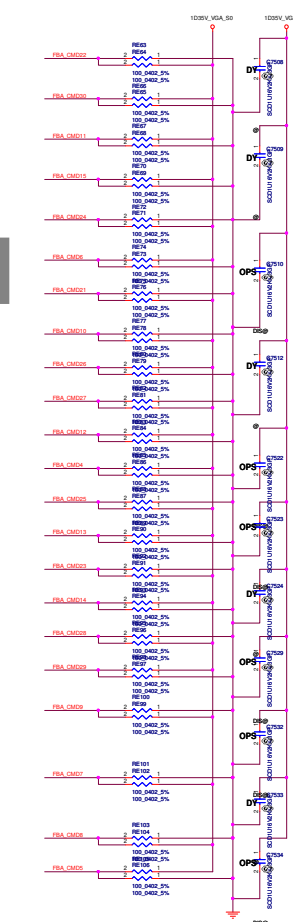


Table 6-4. Mode E Command Mapping

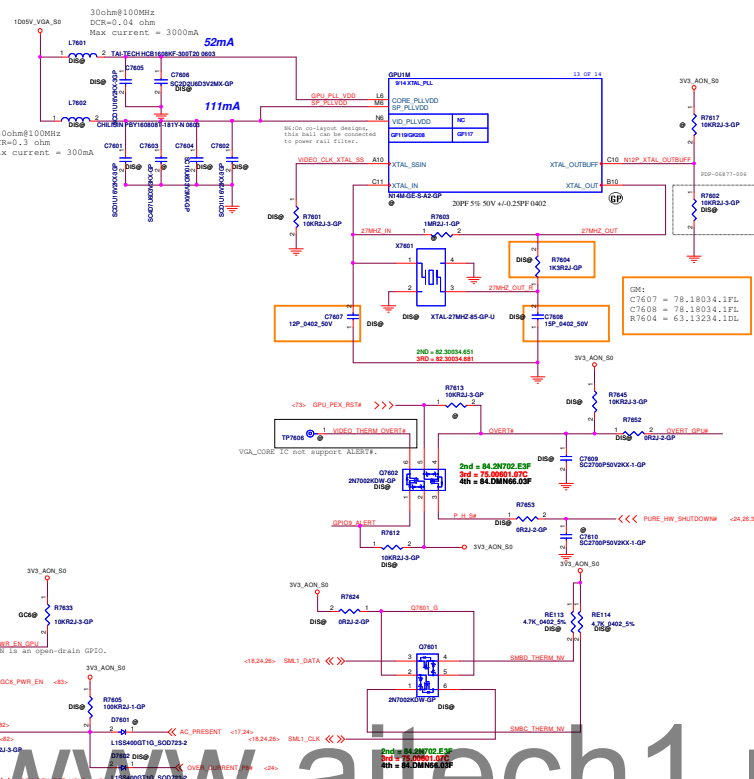
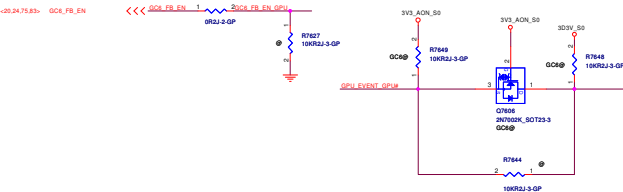
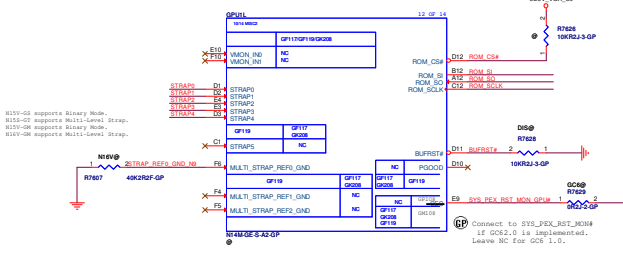
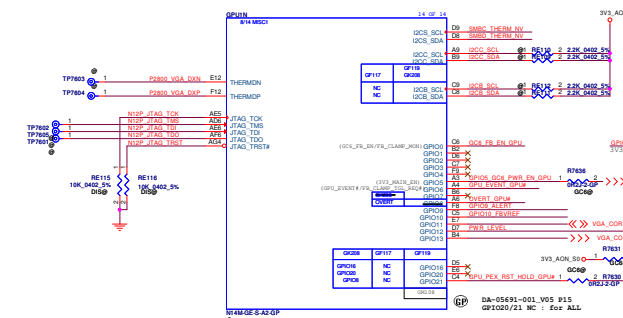
N15x DDR3 Mode E	Rank 0		Rank 1	
	Data Bits [31:0]	Data Bits [63:32]	Data Bits [31:0]	Data Bits [63:32]
Fb _N _CMD0	ODT		ODT	
Fb _N _CMD1			CS1*	
Fb _N _CMD2	CS0*			
Fb _N _CMD3	CKE		CKE	
Fb _N _CMD4	A9	A9	A11	A11
Fb _N _CMD5	A6	A6	A7	A7
Fb _N _CMD6	A3	A3	BA1	BA1
Fb _N _CMD7	A0	A0	A12	A12
Fb _N _CMD8	A8	A8	A8	A8
Fb _N _CMD9	A12	A12	A0	A0
Fb _N _CMD10	A1	A1	A2	A2
Fb _N _CMD11	RA5*	RA5*	RA5*	RA5*
Fb _N _CMD12	A13	A13	A14	A14
Fb _N _CMD13	BA1	BA1	A3	A3
Fb _N _CMD14	A14	A14	A13	A13
Fb _N _CMD15	CA5*	CA5*	CA5*	CA5*
Fb _N _CMD16		ODT		ODT
Fb _N _CMD17				CS1*
Fb _N _CMD18		CS0*		
Fb _N _CMD19		CKE		CKE
Fb _N _CMD20	RST	RST	RST	RST
Fb _N _CMD21	A7	A7	A6	A6
Fb _N _CMD22	A4	A4	A5	A5
Fb _N _CMD23	A11	A11	A9	A9
Fb _N _CMD24	A2	A2	A1	A1
Fb _N _CMD25	A10	A10	WE*	WE*
Fb _N _CMD26	A5	A5	A4	A4
Fb _N _CMD27	BA2	BA2		
Fb _N _CMD28	WE*	WE*	A10	A10
Fb _N _CMD29	BA0	BA0	BA0	BA0
Fb _N _CMD30			BA2	BA2
Fb _N _CMD31				
Fb _N _CMD32				
Fb _N _CMD33 ¹				

Table 3-9. DDR3 GPU-side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type	Footprint	Population	Location
GB25-64 DDR3	0.1 μ F	X7R 0402	2 2	Under GPU
	1 μ F	X7R 0603	2 2	Under GPU
	4.7 μ F	X6S 0603	2 2	Under GPU
	10 μ F	X5R 0805	1 1	Near GPU
	22 μ F	X5R 0805	1 1	Near GPU

GPU Package	PLL Rail	Capacitor Type		Footprint	Population	Location
GB2B-64 and GB4B-128	PLLVD	0.1 μ F	X7R	0402	1	Under GPU
		22 μ F	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.05)		0402	1	Near GPU

GPU Package	PLL Rails	Capacitor Type	Footprint	Population	Location
GB2B-64	SP_PLLVDD +	0.1 μ F X7R	0402	1 per ball	Under GPU
GB4B-128	VID_PLLVDD	4.7 μ F X5R	0603	1	Near GPU
GB3-256		22 μ F X5R	0805	1	Near GPU
Bead Type					
		180 Ω (ESR=0.2)	0603	1	Near GPU



		Strap	
128Mx16 DDR3L	Hynix	0x9	H5TC2G63FFR-11C
	Micron	0xA	MT41J128M16JT-093G:K
	Samsung	0xB	K4W2G1646E-BY11
256Mx16 DDR3L (4 pcs VRAM)	Hynix	0x3	H5TC4G63AFR-11C
	Micron	0x4	MT41J256M16HA-093G:E
	Samsung	0x5	K4W4G1646D-BC1A
256Mx16 DDR3L (8 pcs VRAM)	Hynix	0xC	H5TC4G63AFR-11C
	Micron	0xD	MT41J256M16HA-093G:E
	Samsung	0xE	K4W4G1646D-BC1A

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

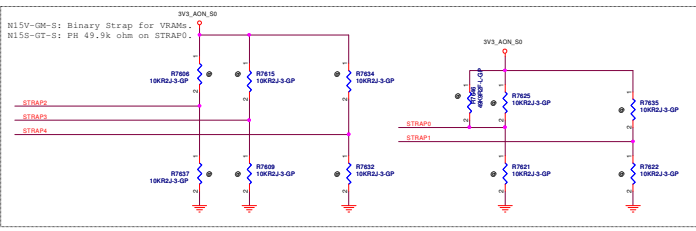


Table 9. N15V-GM Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10kΩ	Pull-down to GND
ROM_SEN1	SMB_VEHND0	10kΩ	<ul style="list-style-type: none"> +Pull-up to 3V3 if VBIOS ROM exists +Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10kΩ	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10kΩ	See note below
STRAP1	RAM_CFG[1]	10kΩ	See note below
STRAP2	RAM_CFG[2]	10kΩ	See note below
STRAP3	RAM_CFG[3]	10kΩ	See note below
STRAP4	PCIE_MAX_SPEED	10kΩ	Pull-down to GND

		Strap	STRAP3	STRAP2	STRAP1	STRAP0	
128Mx16 DDR3L	Hynix	0xC	H5TC2G63FFR-11C	1	1	0	0
	Micron	0x1	MT41K128M16JT-107G:K	0	0	0	1
	Samsung	0x5	K4W2G1646E-BY11	0	1	0	1
256Mx16 DDR3L	Hynix	0x4	H5TC4G63AFR-11C	0	1	0	0
	Micron	0xD	MT41K256M16HA-107G:E	1	1	0	1
	Samsung	0x9	K4W4G1646D-BC1A	1	0	0	1

Table 10. Multi-Level Strap Differences

Physical Strapping Pin	GPU	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping
ROM_SCLK	H1155-GV	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EXT_ERL
		H1155-GM/-GT	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	ALL GB2-64 H1155-GM/-GT GB2-64 H115	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	H1155-GV	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
	H1155-GM/-GT	DEVID_SEL	PCIE_CFG		
STRAPO	H1155-GV	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	H1155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and stuff 50kΩ pull-up)			
	H1155-GV	3G0_PADCFG[3]	3G0_PADCFG[2]	3G0_PADCFG[1]	3G0_PADCFG[0]
	H1155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP2	H1155-GV	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
	H1155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP3	H1155-GV	SOR2_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
	H1155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP4	H1155-GV	RESERVED	PCIE_SPEED_CHA_HGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD033V
	H1155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

	N15V-GM	N155-GT
Chip	N15V-GM	N155-GT
Device ID	0x1140	0x1341
Memory Interface	sDDR3	SDDR3
Package	595 ball BGA 23x23mm	595 ball BGA 23 x 23 mm 908 ball BGA 29 x 29 mm

Table 3-6. NVVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type		Footprint	Population	Location	Comments
GB2B-64	4.7 μ F	X6S	0603	10	10	Under GPU
	1 μ F	X6S	0402	4	4	Under GPU
	47 μ F	X5R	0805	1	1	Near GPU
	22 μ F	X5R	0805	1	1	Near GPU
	4.7 μ F	X5R	0805	5	5	Near GPU
	330 μ F	POS	7343	1	1	Near GPU ESR \leq 6 m Ω

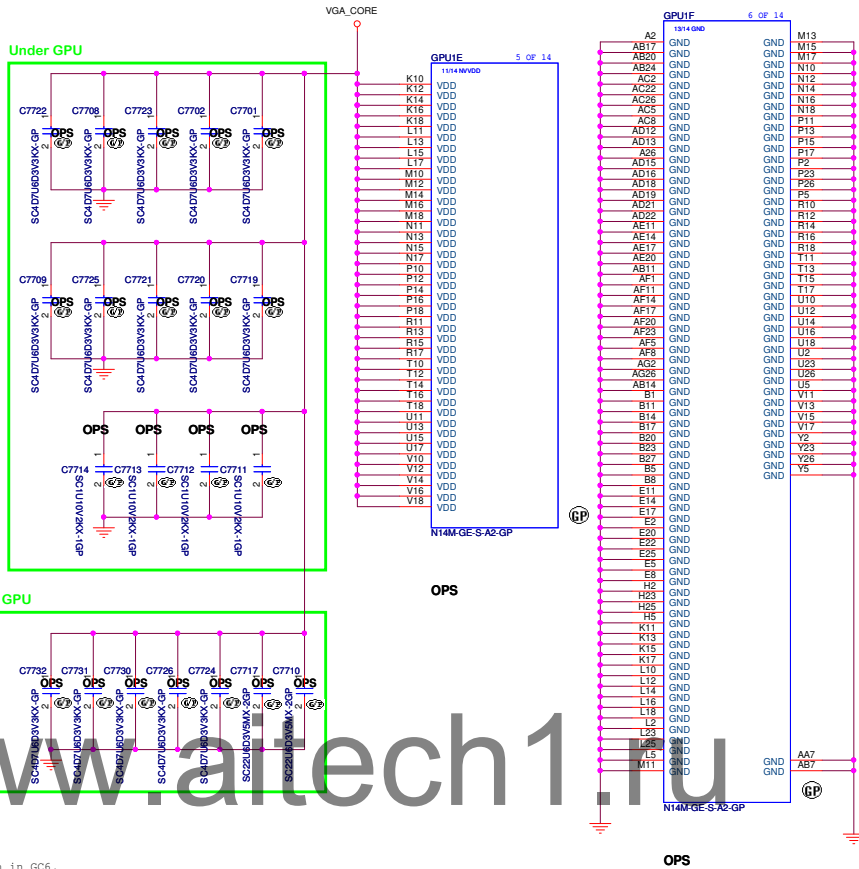
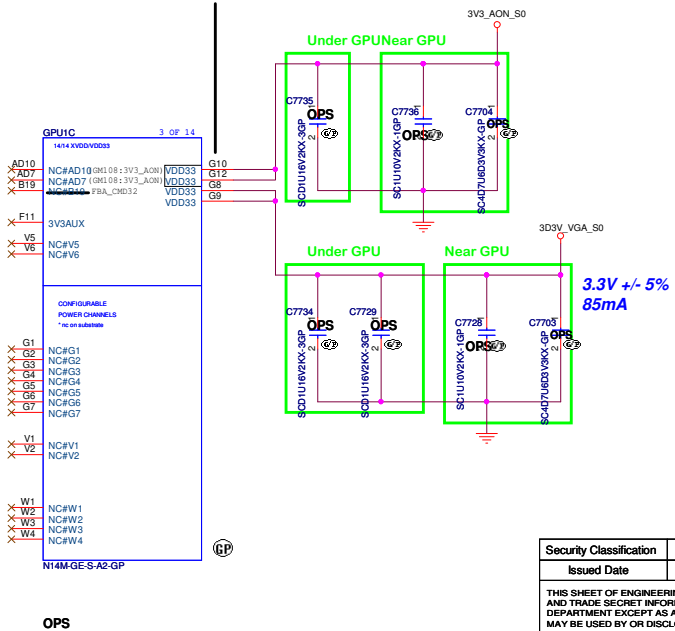


Table 3-27. 3.3V Power Rail Decoupling

GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64	3V3_MAIN	0.1 μ F	X6S	0402	2
GB4B-128		1 μ F	X5R	0603	1
GB3-256		4.7 μ F	X5R	0603	1
GB2B-64	3V3_AON	0.1 μ F	X6S	0402	1
GB4B-128		1 μ F	X5R	0603	1
GB3-256		4.7 μ F	X5R	0603	1

Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.

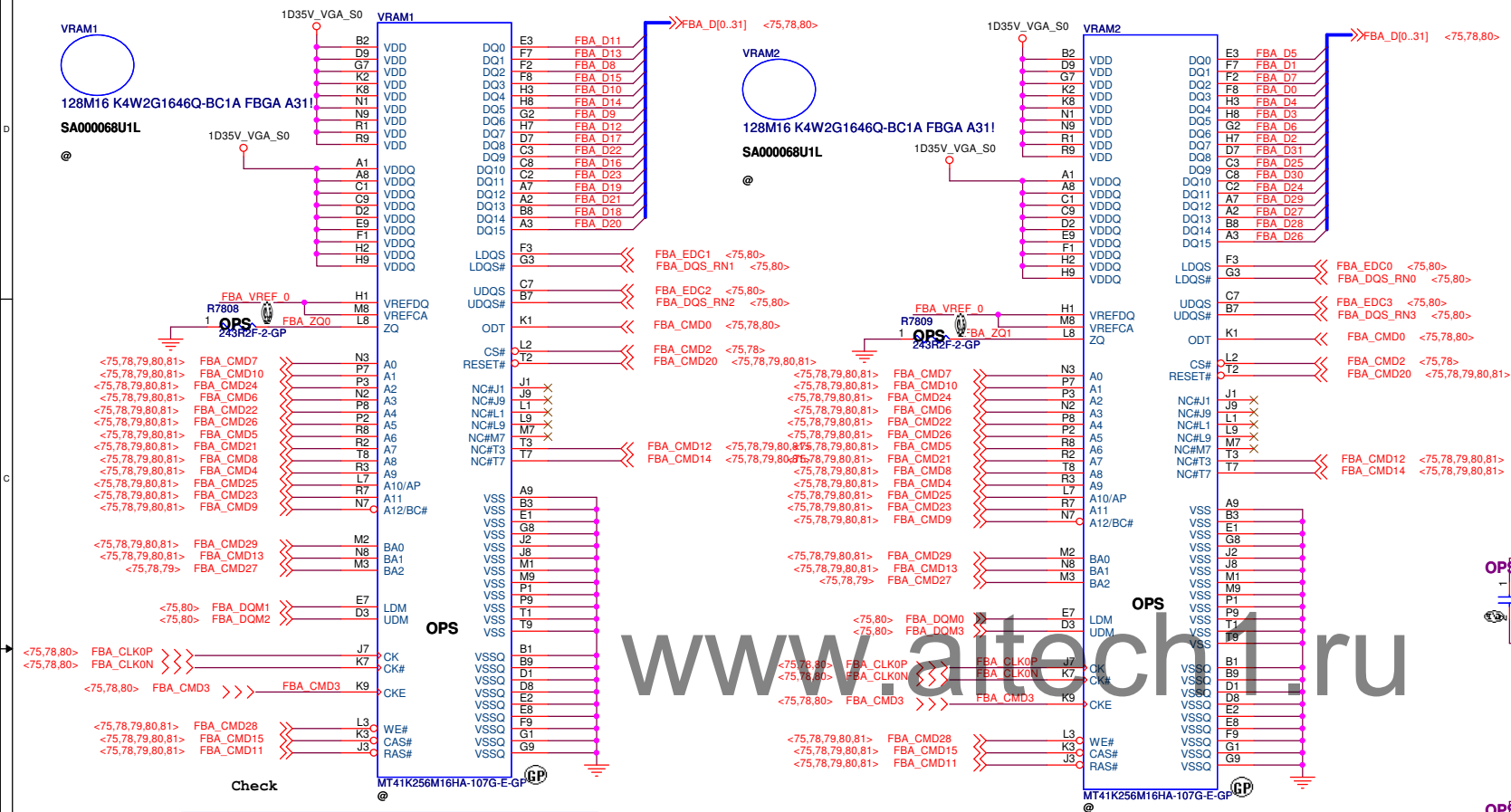
G10, G12:
If GC62.0 is implemented, connect to a 3V3 rail that will be on in GC6.
If GC62.0 is NOT implemented, connect to the same rail as VDD33.



1GB, Single Rank, 4 pcs VRAM							
GPU	GPU DPN	Memory Vendor	2Gb DDR3L:(1.35v/900Mhz)	DPN	WPN	Voltage	Note
IC VGA N15V-GM-S-A2 GB2-64 FCBA595P	JG0YH	Hynix	H5TC263FFR-11C	X1PRC	72.52G63.N0U	1.35V	
		Samsung	K4W2G1646Q-BC1A	D0DP7	072.2G164.0A0U	1.35V	
		Micron	MT41K128M16JT-107G-K	HKKF2	72.41128.N0U	1.35V	
2GB, Single Rank, 4 pcs VRAM							
GPU	GPU DPN	Memory Vendor	4Gb DDR3L:(1.35v/900Mhz)	DPN	WPN	Voltage	Note
IC VGA N15V-GM-S-A2 GB2-64 FCBA595P	JG0YH	Hynix	H5TC4G63AFR-11C	021N2	72.05463.D0U	1.35V	Build in EVT
		Samsung	K4W4G1646D-BC1A	07XGT	072.4G164.0A0U	1.35V	
		Micron	MT41K256M16HA-107G-E	R5RH5	72.41K26.00U	1.35V	Build in EVT
4GB, Dual Rank, 8 pcs VRAM							
GPU	GPU DPN	Memory Vendor	4Gb DDR3L:(1.35v/900Mhz)	DPN	WPN	Voltage	Note
IC VGA N15S-GT-S-A2 GB2-64 FCBA595	PXP79	Hynix	H5TC4G63AFR-11C	021N2	72.05463.D0U	1.35V	Build in EVT
		Samsung	K4W4G1646D-BC1A	07XGT	072.4G164.0A0U	1.35V	
		Micron	MT41J256M16HA-093G-E	PP8TP	072.41256.080U	1.35V	

Main Func = dGPU

Data Bits 31:0 RANK 0



Place close VRAM1 VDD ball

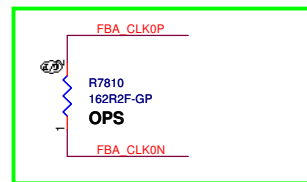
Place close VRAM2 VDD ball

Place close VRAM1VDDQ ball

Place close VRAM2VDDQ ball

Frame Buffer Partition A-Lower Half

FBCLK Termination place on VRAM side



FBVREF Termination

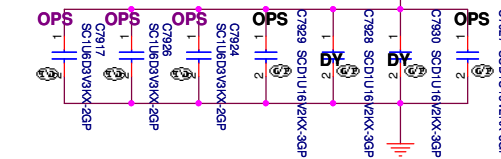
Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population		Location
			FBVDDQ	FBVDD	
FBVDD/Q Combined					
0.1 μF	X7R	0402	2		Under DRAM
1.0 μF	X7R	0603	4		Under DRAM
10 μF	X5R	0805	0		Close to DRAM

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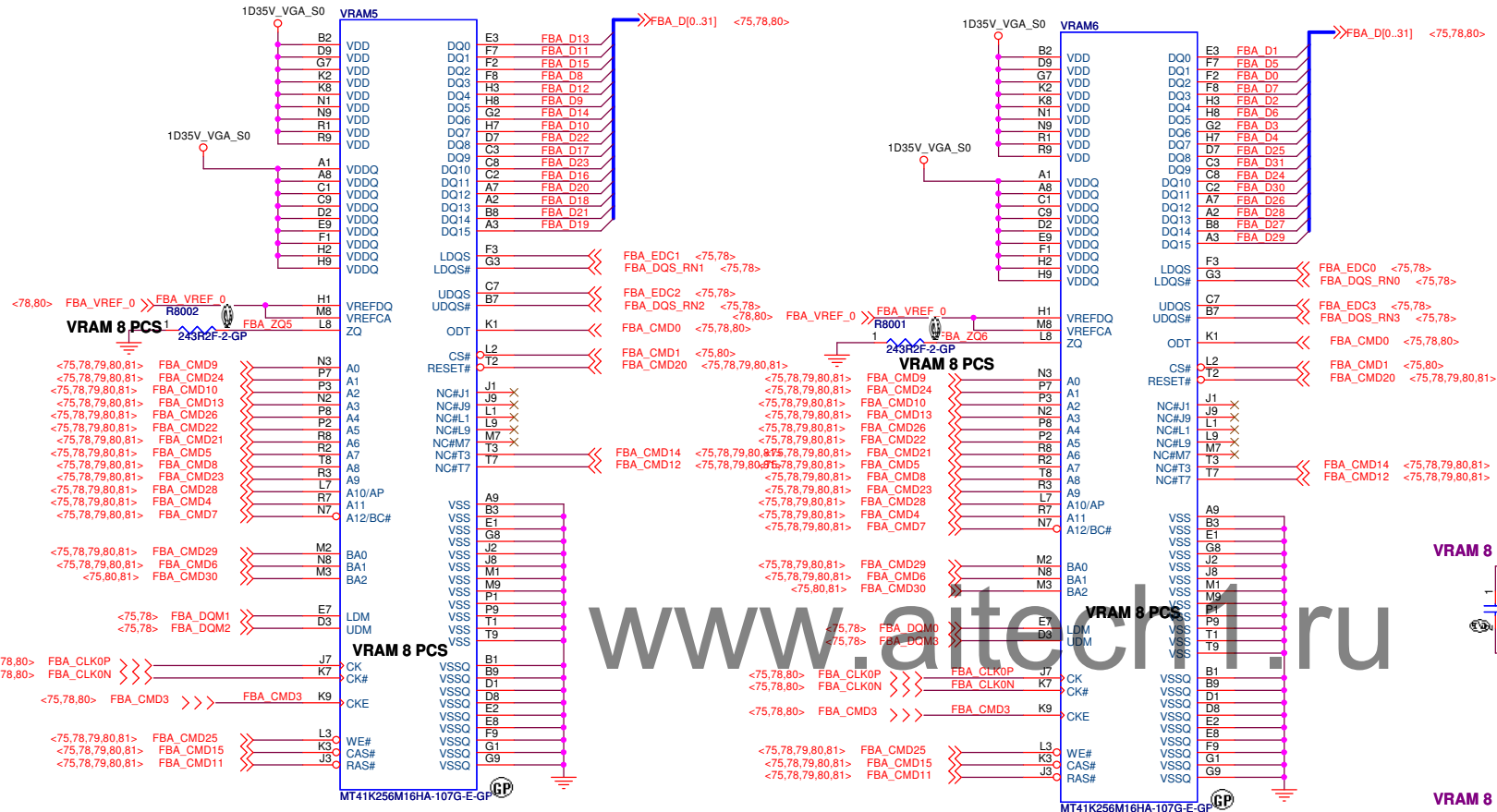
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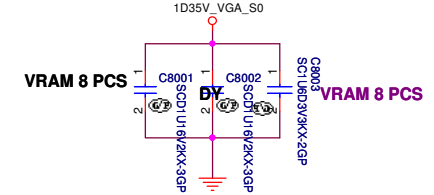
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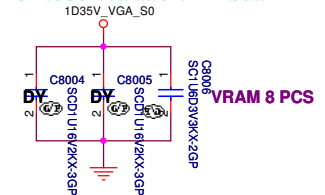
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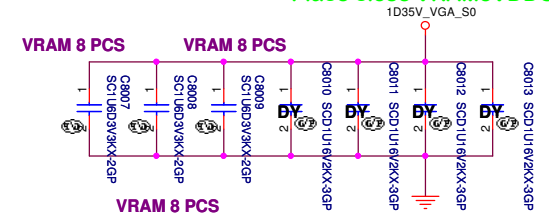
Place close VRAM5 VDD ball



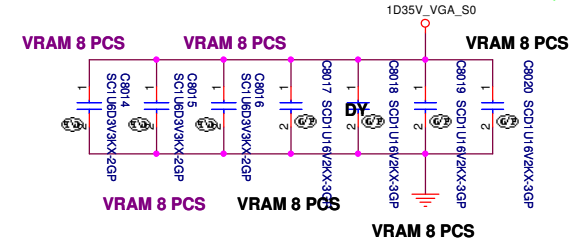
Place close VRAM6 VDD ball



Place close VRAM5VDDQ ball



Place close VRAM6VDDQ ball

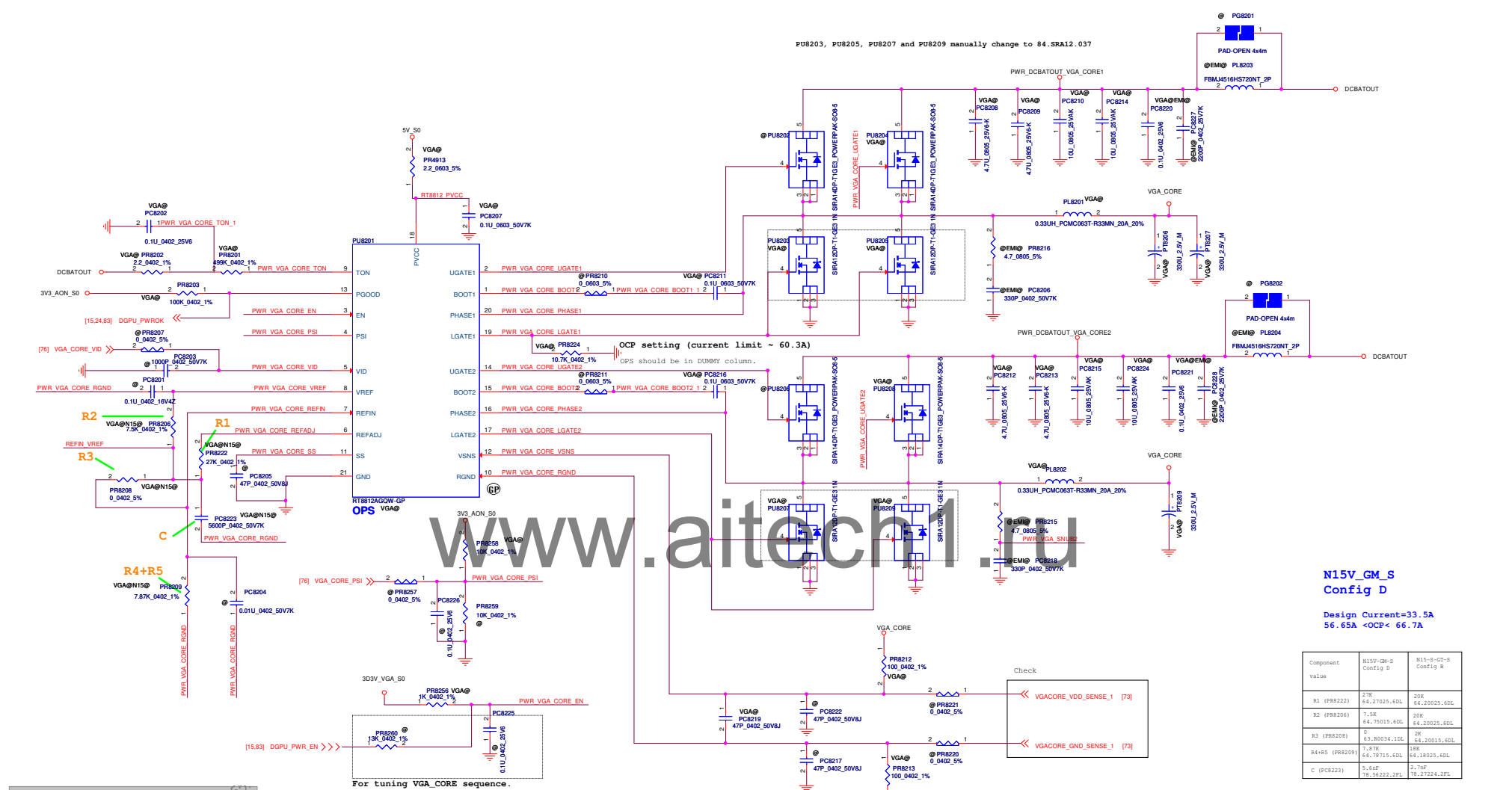


FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

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PUB203, PUB205, PUB207 and PUB209 manually change to 84.SRA12.037



N15V_GM_S
Config D

Design Current=33.5A
56.65A <OCP< 66.7A

Component	N15V-GM-S Config D	N15-S-QT-S Config A
R1 (PR8222)	27K 64.27025,60L	20K 64.20025,60L
R2 (PR8206)	7.5K 64.75015,60L	20K 64.20025,60L
R3 (PR8208)	0 63.80034,10L	2K 64.20015,60L
R4+R5 (PR8209)	7.87K 64.78715,60L	10K 64.10025,60L
C (PC8223)	5.6nF 78.56222,20L	2.7nF 78.27024,20L

78.56222,20L:OBS NEARON: 50V is more popular, change to 78.56224,20L

PWM-VID Specification				
	Config A	Config B	Config C	Config D
Vmin	0.6	0.6	0.6	0.9
Vmax	1.2	1.2	1.15	1.15
Vboot	0.875	0.9	0.9	1.025
Voltage Step Vstep	mV 6.25	6.25	25	12.5
Number of Voltage Levels N	96	96	20	20
PWM Frequency F _{PWM}	MHz 1.125	0.676	0.676	
PWM Minimum Pulse Width T _{min}	ns 9.26	74	74	
VID Transient Time T	<100	<100	<100	
Component Value				
R1 (R1)	KQ 39	20	39	27
R2 (R1)	KQ 39	20	30	7.5
R3 (R1)	KQ 1.5	2	3	0
R4 (R1)	KQ 30	18	24	6.2
R5 (R1)	KQ 1.5	0	3	1.74
C	nF 1.5	2.7	1.8	5.6

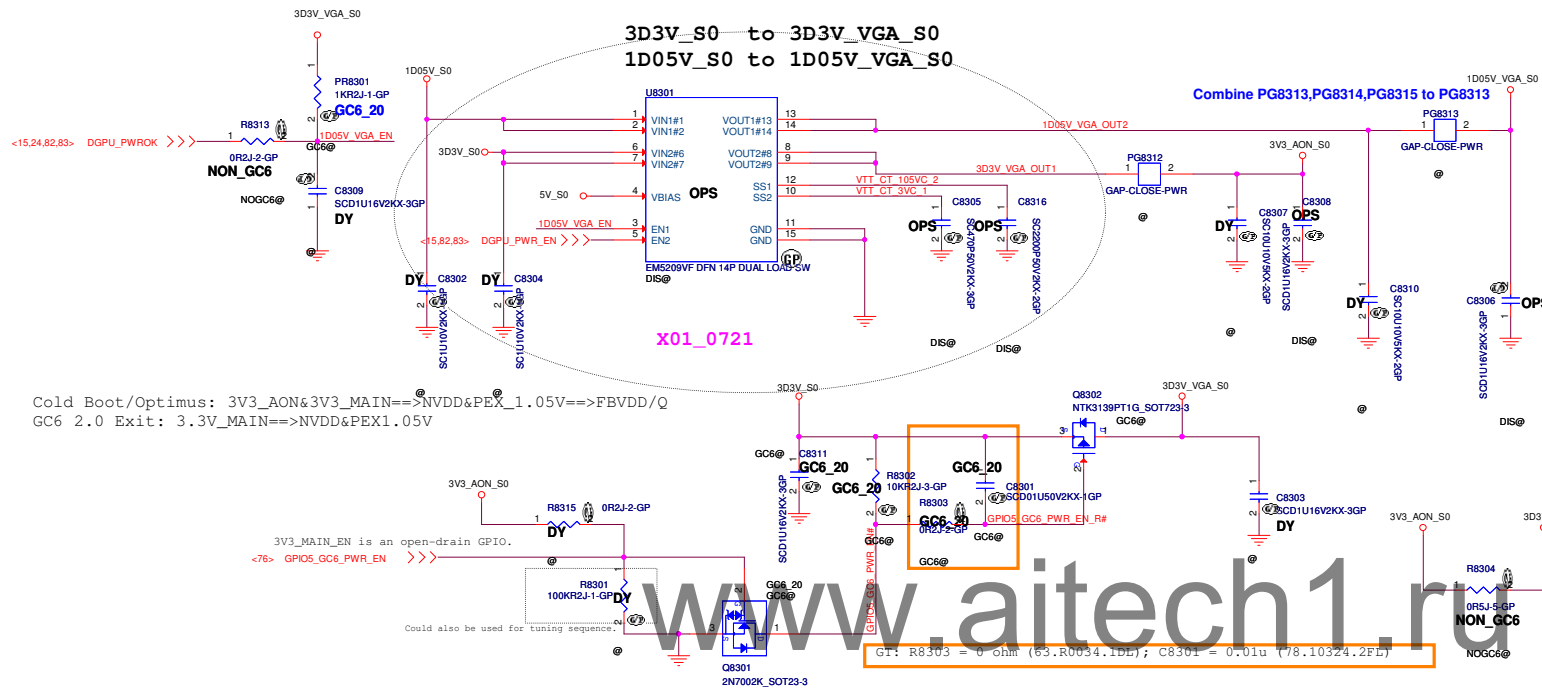


I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor:CHIP CHOKE 0.22UH PCMC104T-R22/ 1mohm/ Isat =60A rms /68.R2210.10C
O/P cap: CHIP CAP EL 330U 2.5V M6.3*4.4 Chemi-con/79.3371V.6CL
H/S: SIRA14DP-T1-GE3 / 6.8mohm/8.5mOhm@4.5Vgs/ 84.A14DP.037
L/S:SIRA06DP-T1-GE3 / 2.75mohm/3.5mOhm@4.5Vgs/ 84.SRA06.037

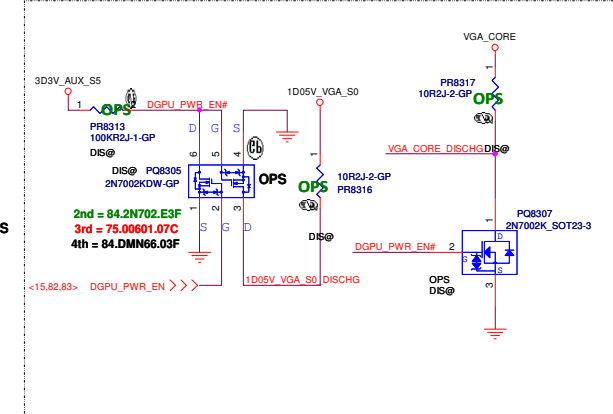
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3D3V_VGA_S0
1D05V_VGA_S0

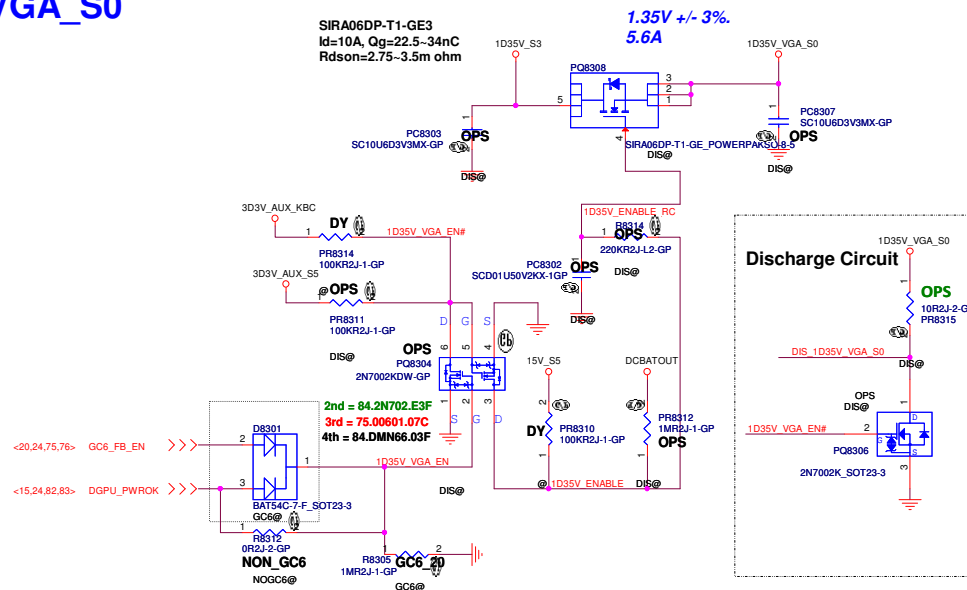
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3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D35V_VGA_S0 should ramp-up before 1D05V_VGA_S0
```



VGA_CORE&1D05V_VGA_S0 Discharge Circuit



1D35V_VGA_S0



CTx (pF)	Rise Time (μs) 10% - 90%, COU = 0.1μF @ VIN; VOUT=0 ohm load							
	Typical values @ 25°C, 25V X7R 10% ceramic cap							
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	1V	0.8V
0	107	72	46	41	36	34	33	29
220	425	276	146	122	103	91	88	74
270	489	316	172	139	121	107	104	84
470	774	487	272	224	181	159	154	123
680	1108	708	375	317	242	221	213	168
1000	1561	1007	546	441	364	314	299	234
2200	3600	2289	1240	1019	817	681	665	539
4700	7757	5092	2674	2203	1808	1592	1516	1177
10000	15700	10310	5601	4659	3674	3401	3197	2562

Table 1. Rise time vs. CTx value

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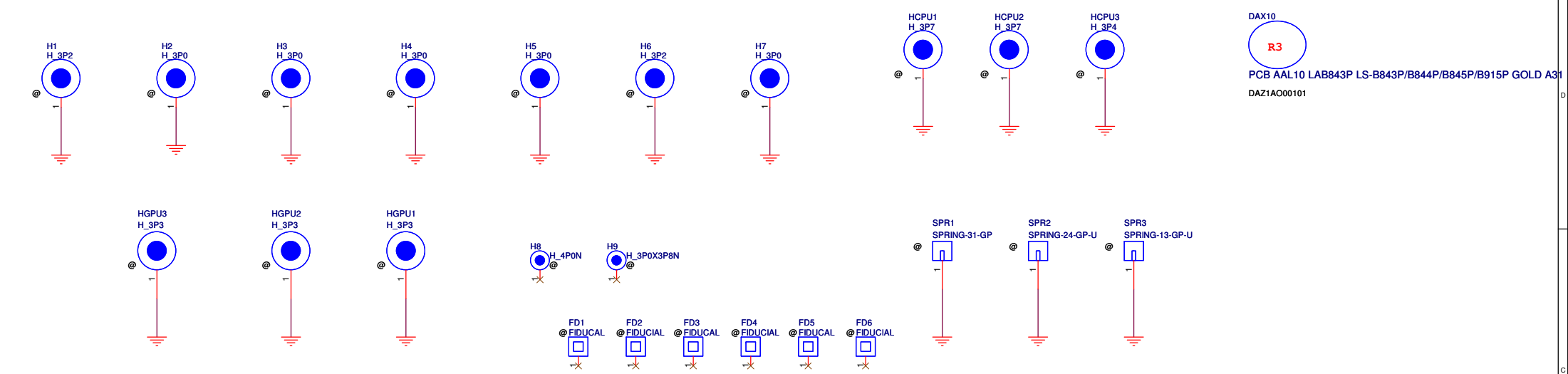
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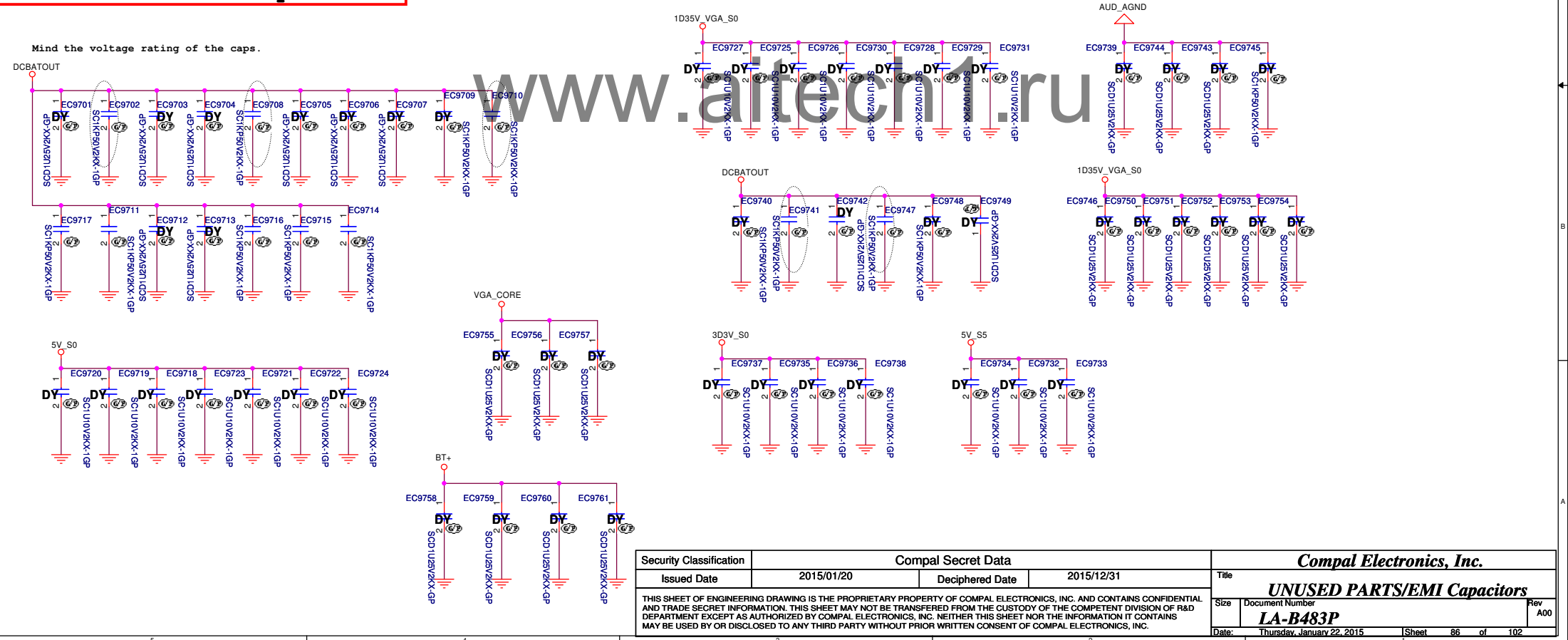
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Main Func = UnusedParts



Main Func = EMICapacitors



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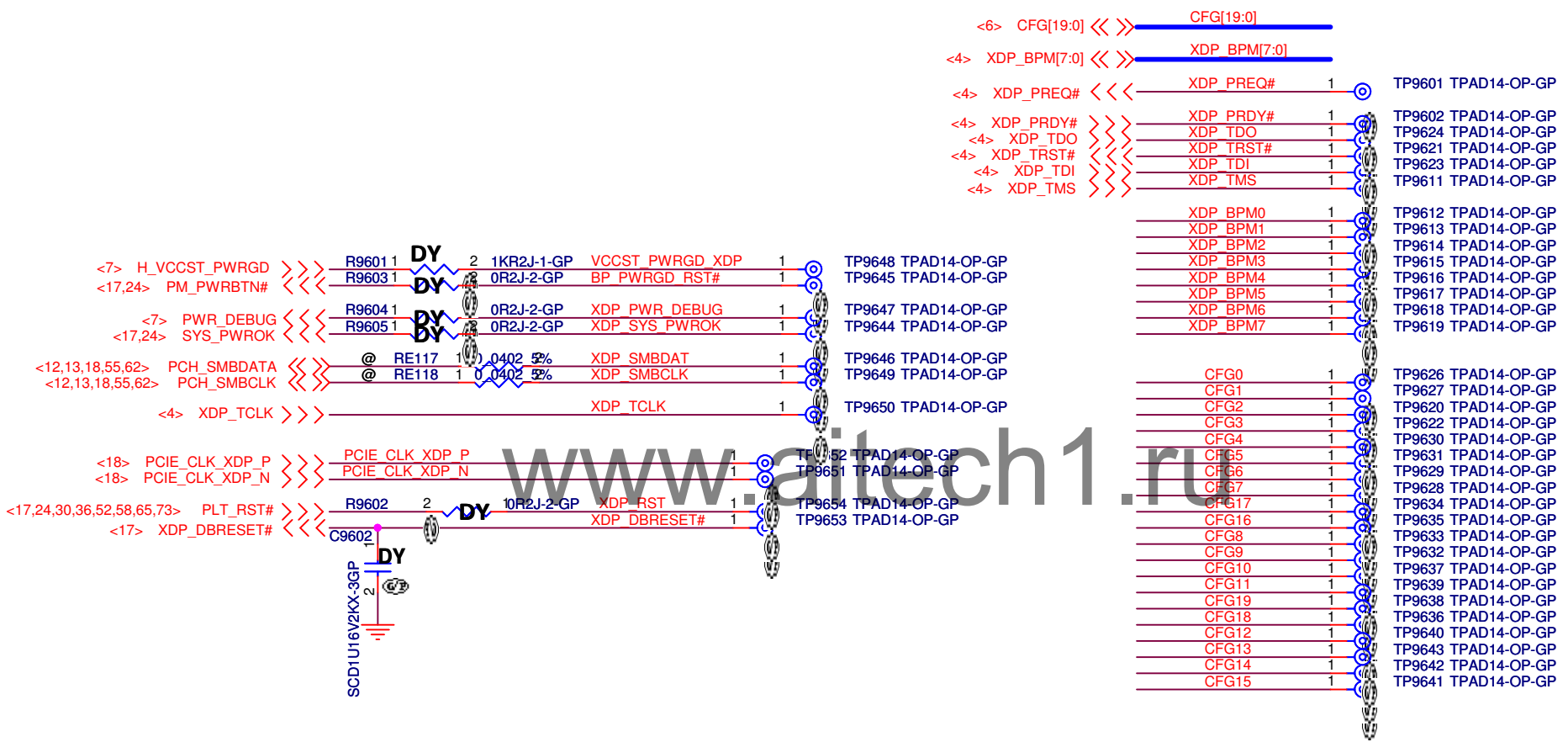
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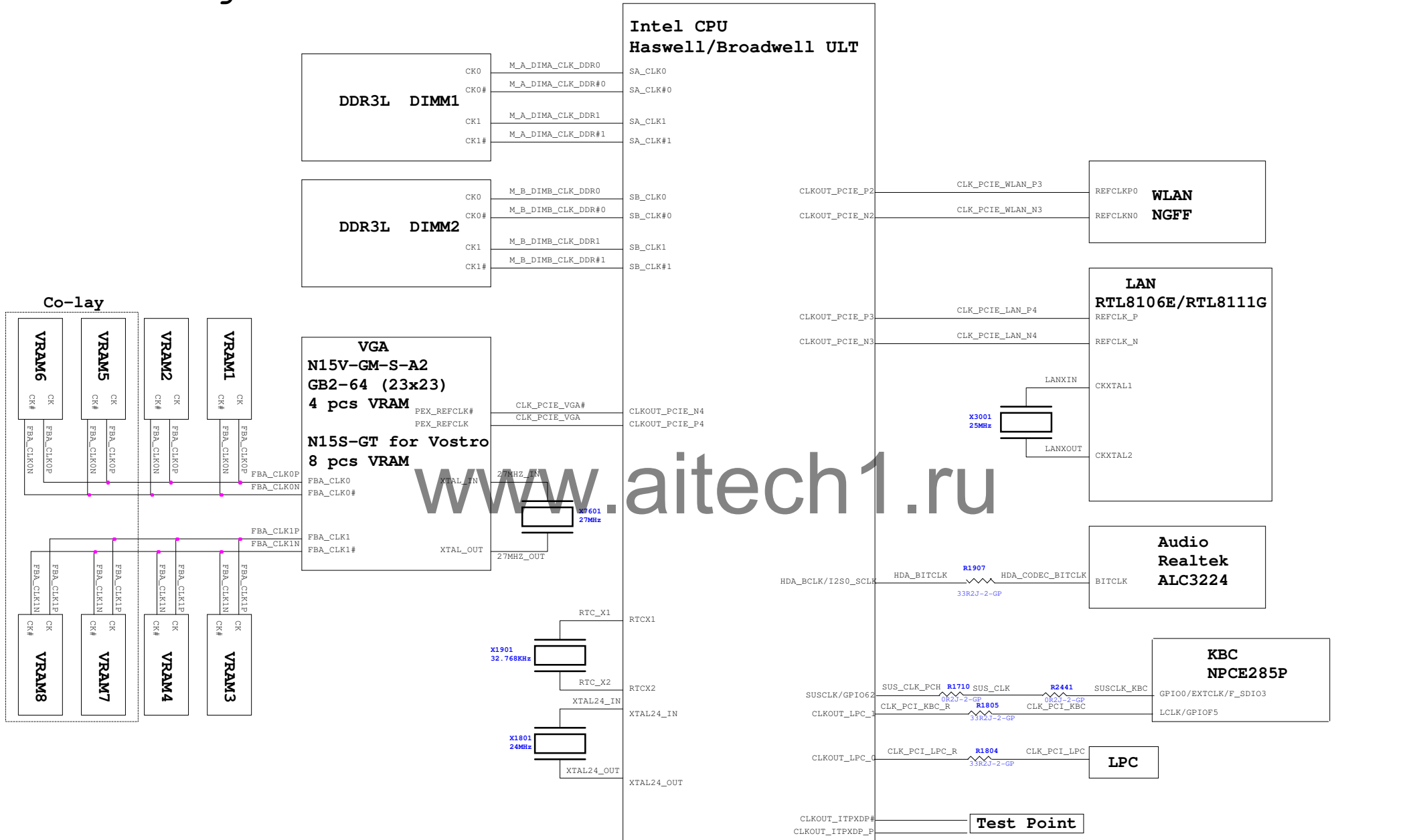
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CPU XDP



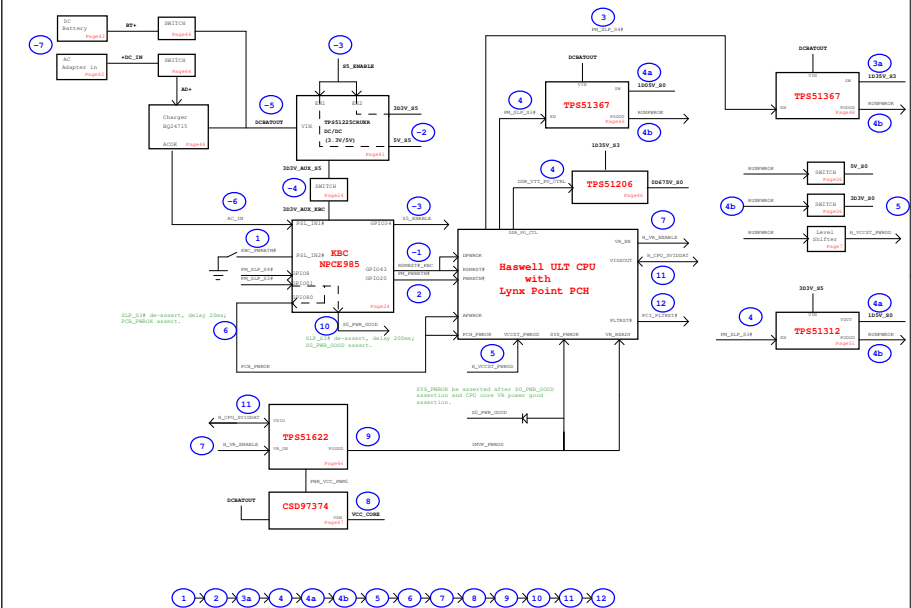
CLK Block Diagram



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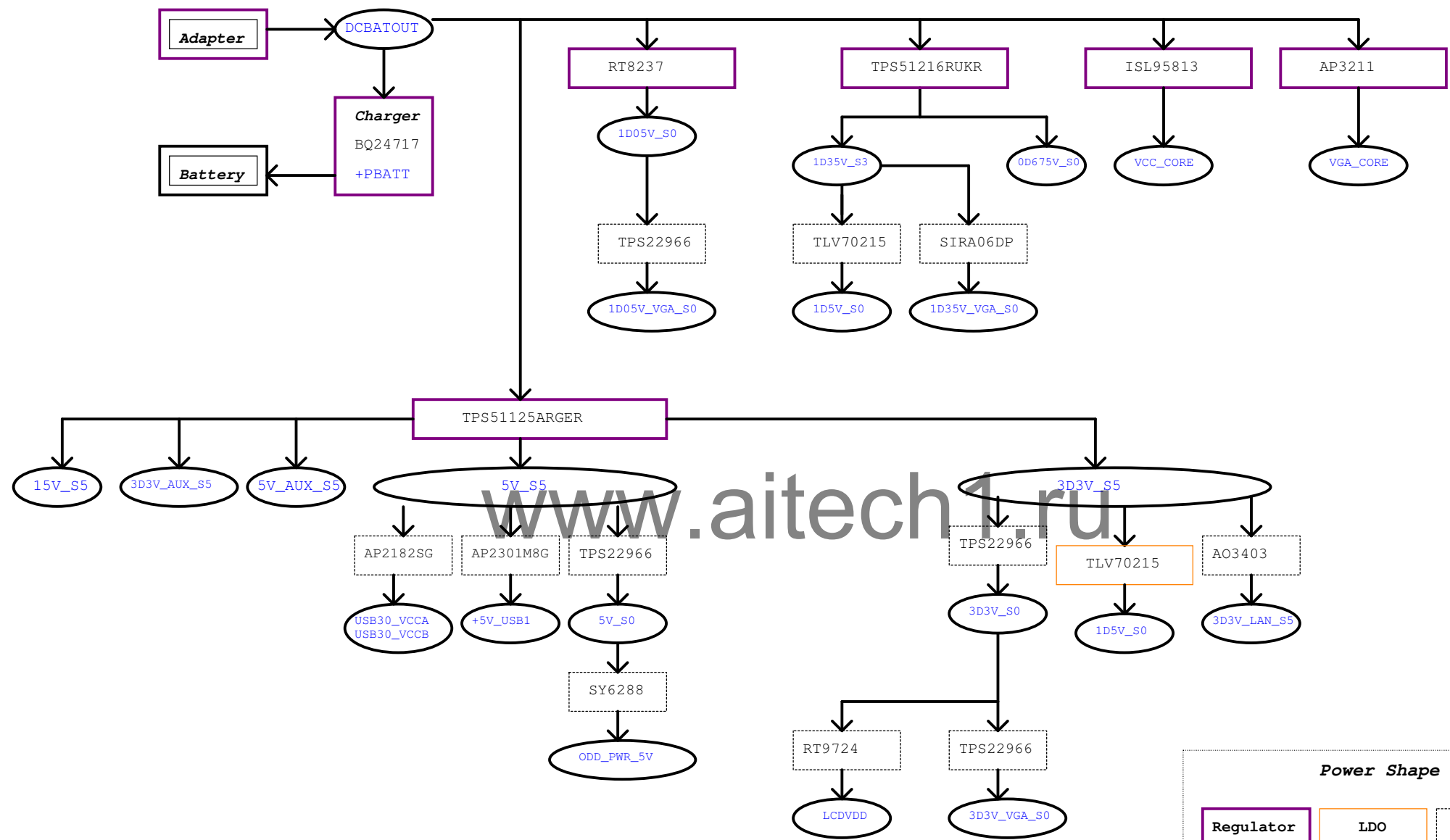
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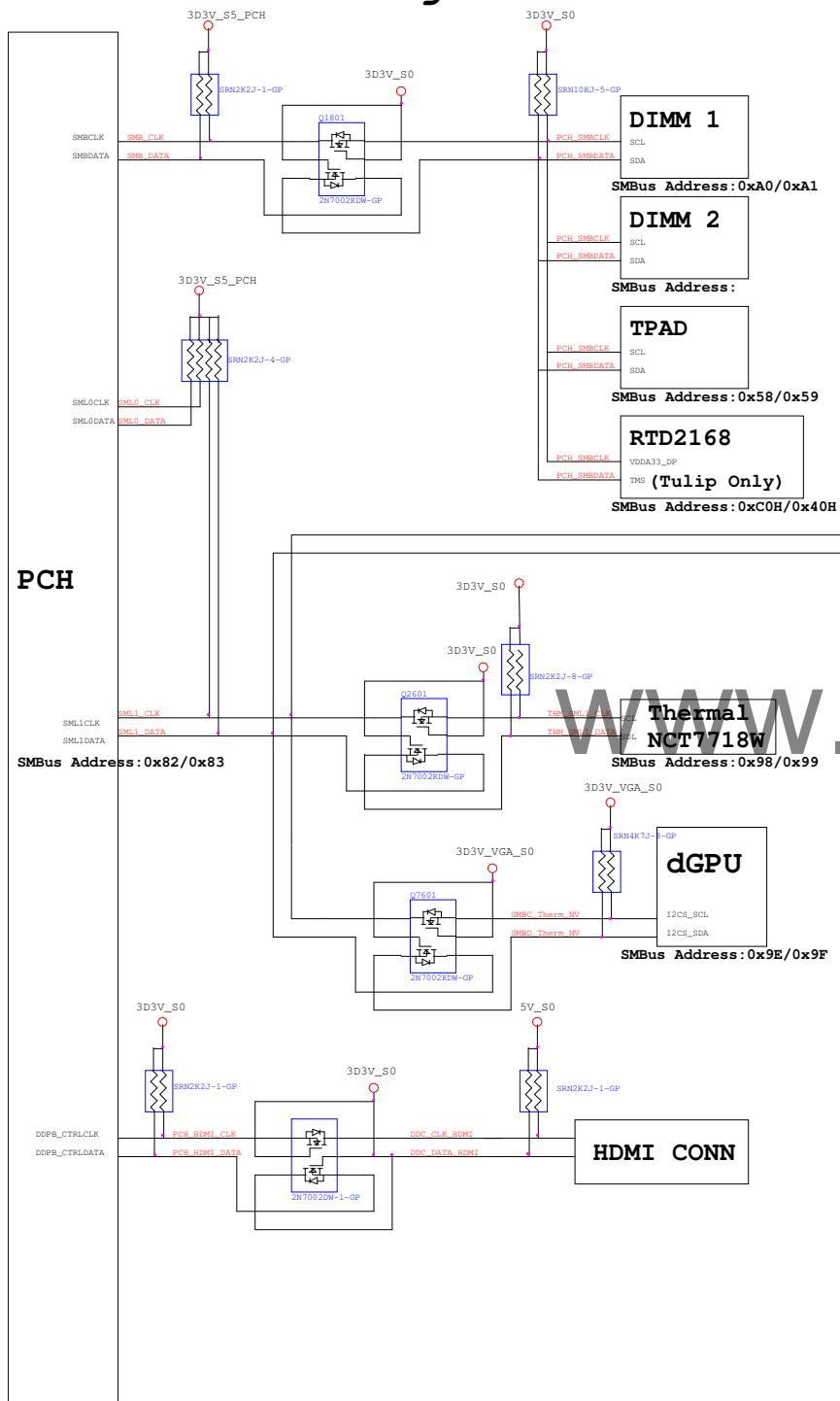


The diagram shows a digital signal transition. A green arrow indicates a delay of 100ns between the input signal and the output signal. The output signal is labeled "PCI to all system outputs".

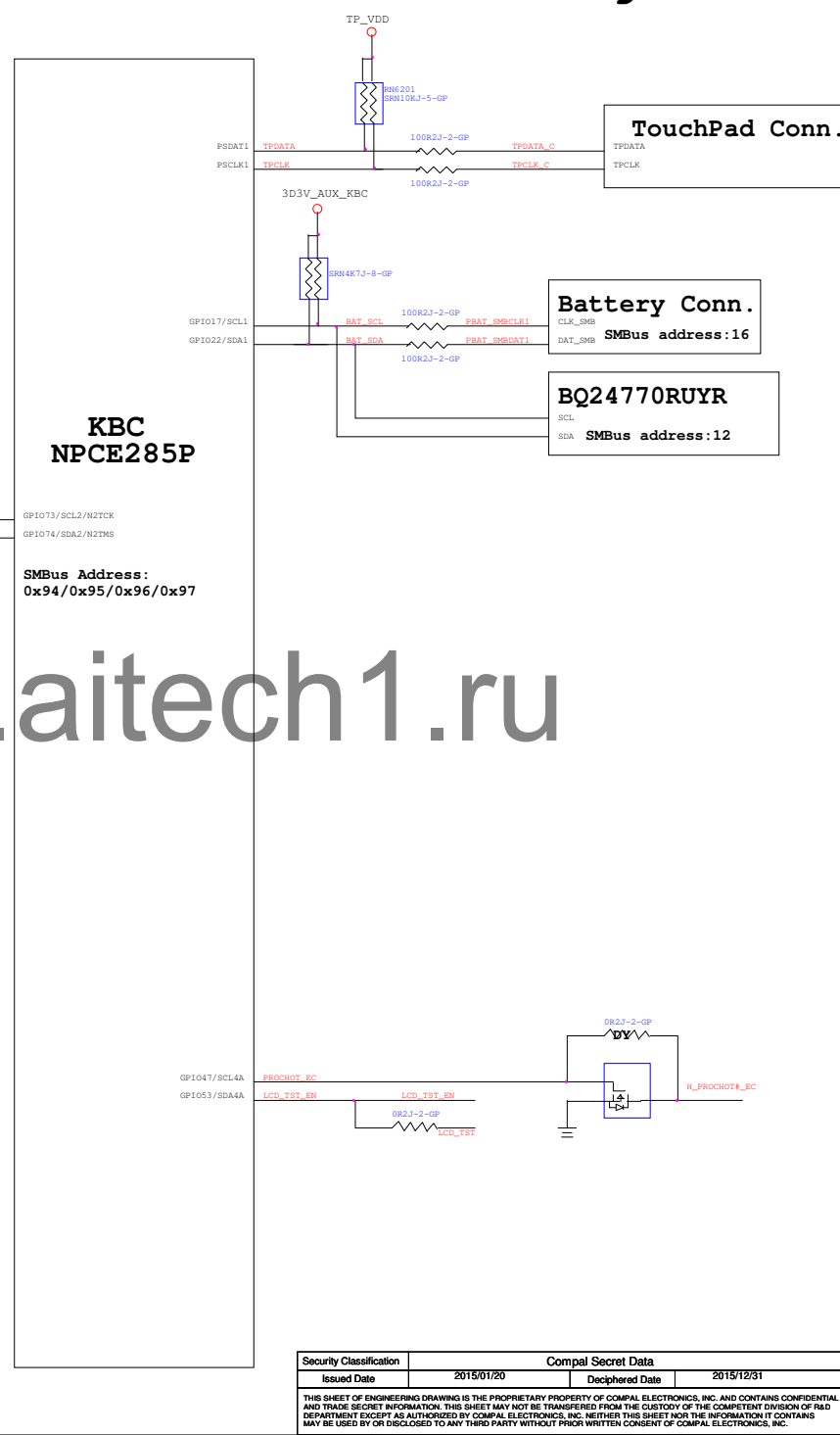
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PCH SMBus Block Diagram

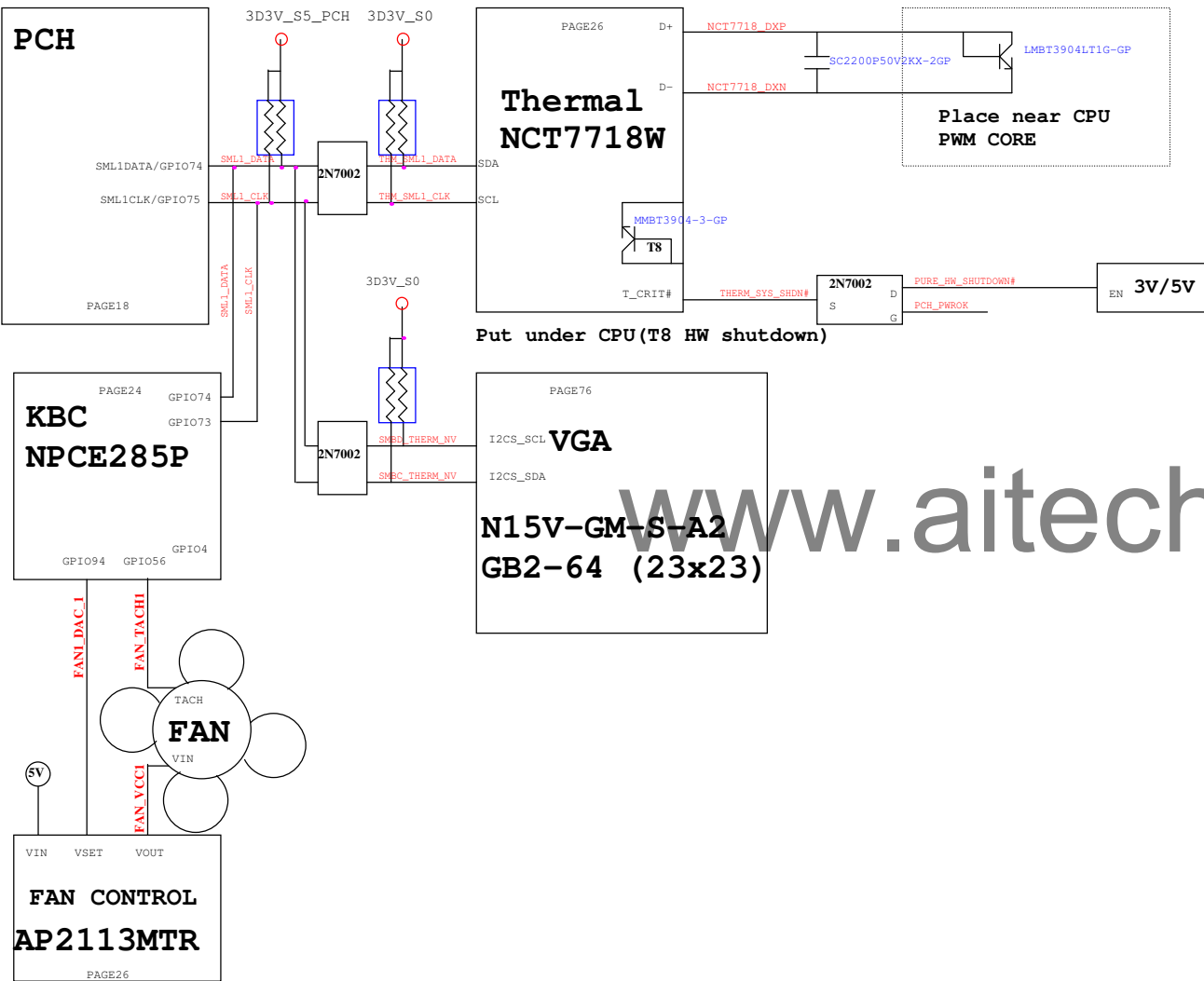


KBC SMBus Block Diagram



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Thermal Block Diagram



Audio Block Diagram

